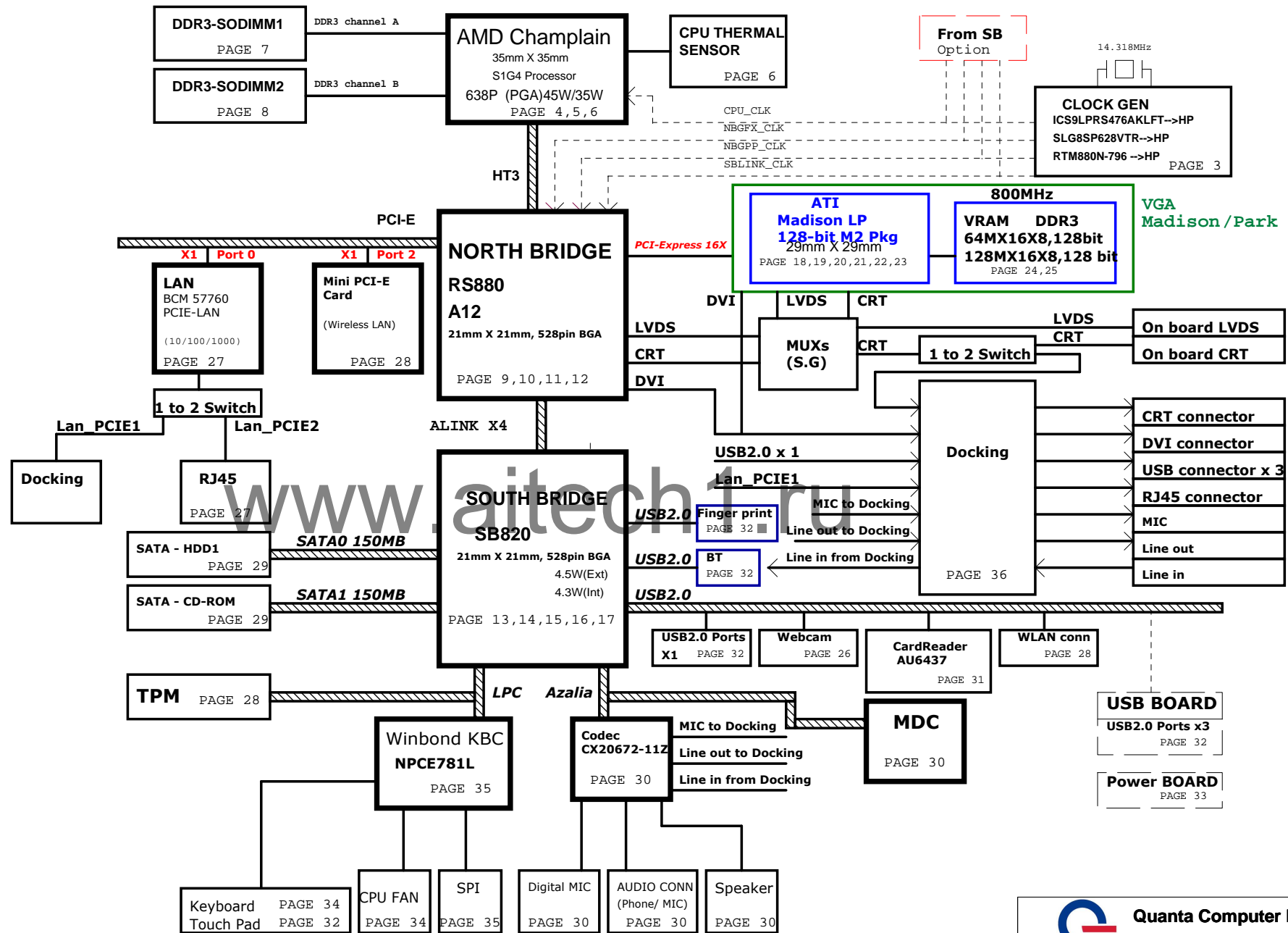


## PCB STACK UP

LAYER 1 : TOP  
LAYER 2 : GND  
LAYER 3 : IN1  
LAYER 4 : IN2  
LAYER 5 : VCC  
LAYER 6 : IN3  
LAYER 7 : GND  
LAYER 8 : BOT

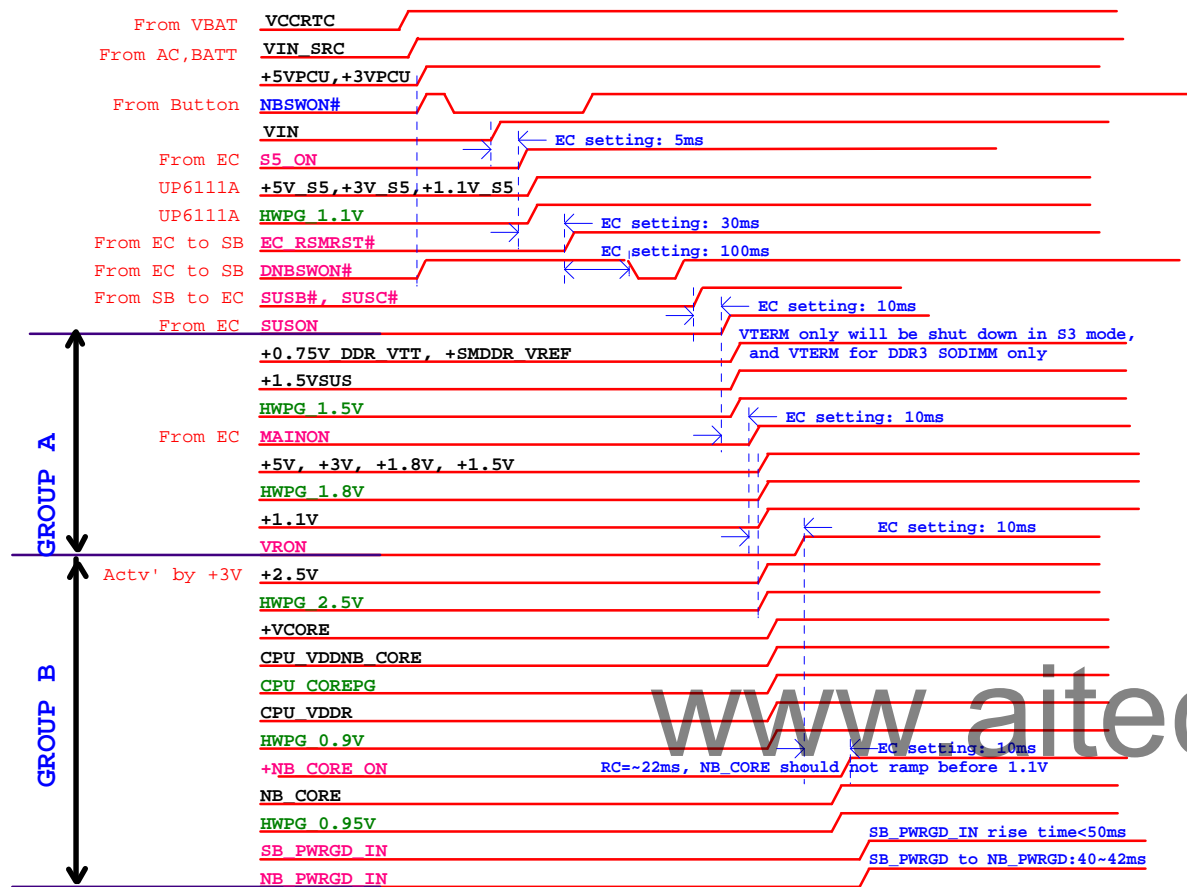
# ZRA SYSTEM DIAGRAM



|                         |         |
|-------------------------|---------|
| AMD CPU CORE (ISL6265)  | PAGE 39 |
| NB_CORE (UP6111AQDD)    | PAGE 41 |
| +VGPU_CORE (MAX8792ETD) | PAGE 43 |
| 1.1V (UP6111AQDD)       | PAGE 40 |
| 1.8V/GPU_Power/+2.5V    | PAGE 44 |
| DDR 1.5V(RT8207)        | PAGE 42 |
| SYSTEM 5V/3V (RT8206)   | PAGE 38 |
| 1V/CPU_VDDR/Discharge   | PAGE 45 |
| Charger (ISL88731)      | PAGE 37 |



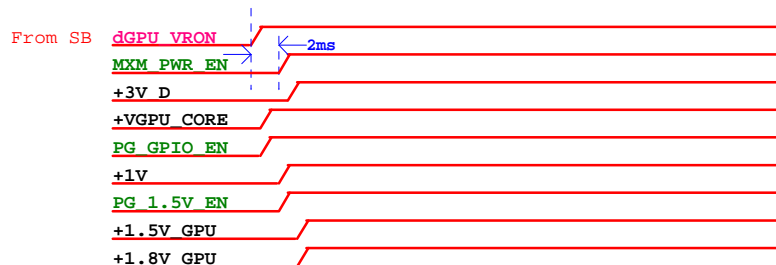
## Danube Power On Sequence



Notice:

- 1.CPU\_LDT\_RST# msut be asserted a minimum of 1ms prior to the assertion of CPU\_PWRGD
- 2.CPU\_CLKP/N must be within specification a minimum of 1ms prior to the assertion of CPU\_PWRGD
- 3.CPU\_PWRGD remains deasserted at least 1ms after both CPU\_CLKP/N and all voltages to the processor are within specification for operation
- 4.all NB power rails(1.8V/1.2V/1.1V) valid before NB\_PWRGD at least 1ms
- 5.stable input clocks from CLKGEN(HT REFCLKP/N) to NB before NB\_PWRGD at least 1ms

## Danube GPU Power Sequence



Power on sequence required:

```
SB800:
1.+3.3V_S5 ramp before +1.1_S5
2.+3.3V ramp before +1.8V
3.+1.8V ramp before +1.1V
4.+3.3V ramp before +1.1V
5.+3.3V_S5 ramping down time>300us
6.All power rails rise time >= 50us, except +3.3V_S5<=40ms
7.100us<=+3.3V_S5 rise time<=40ms
9.VBAT (VCCRTC) must ramp at least 5 seconds before the S5 rails
to allow start time for the internal RTC
```

(only in SB820M NB\_PWRGD signal)  
40ms <= SB PWRGOOD to NB\_PWRGD delay <= 42ms

```
RS880:
1.0<(+3.3V)-(+1.8V)<2.1
2.+1.8V ramp before +1.1V
3.+1.1V ramp before CPU VDDNB CORE
```

## BOM naming rule

| Items | Function           | Name | Description |
|-------|--------------------|------|-------------|
| 1     | Internal CLK GEN   | SGN@ |             |
| 2     | External CLK GEN   | GN@  |             |
| 3     | iGPU               | IV@  |             |
| 4     | dGPU               | SW@  |             |
| 5     | iGPU & dGPU notice | SP@  |             |

### SB SMBUS Table

|                         |         |     |                  |
|-------------------------|---------|-----|------------------|
|                         | CLK GEN | RAM | Mini Card (WLAN) |
| (SB_DA0)/(SB_CL0) (+3V) | V       | V   | V                |
| Power Plane             | +3V     | +3V | +3V              |
| MOS CKT (Level shift)   | X       | X   | X*               |

\*Reserve: There is not SMBUS function in AVL

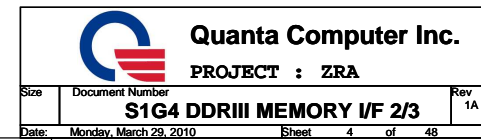
## EC SMBUS Table

|                            |         |                    |
|----------------------------|---------|--------------------|
|                            | Battery | CPU thermal Sensor |
| EC775 SDA1 / SCL1 (+3VPCU) | V       |                    |
| EC775 SDA2 / SCL2 (+3V)    |         | V                  |
| EC775 SDA3 / SCL3 ( )      |         |                    |
| Power Plane                | +3VPCU  | +3V                |
| MOS CKT (Level shift)      | X       | X                  |

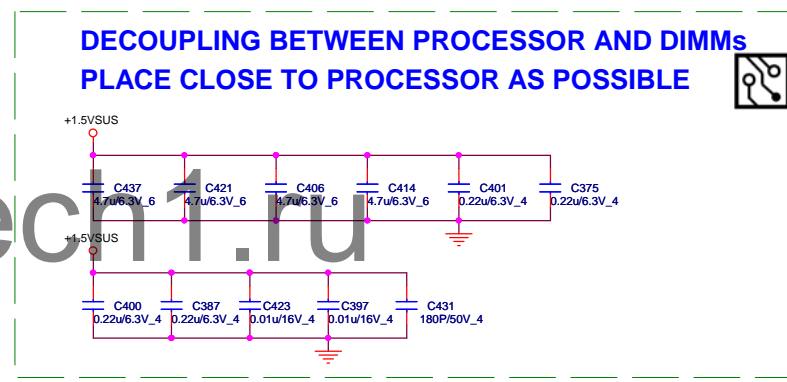
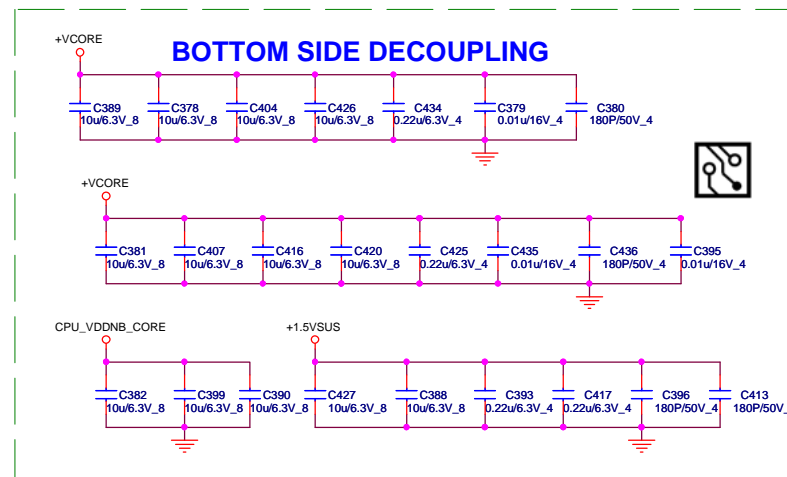
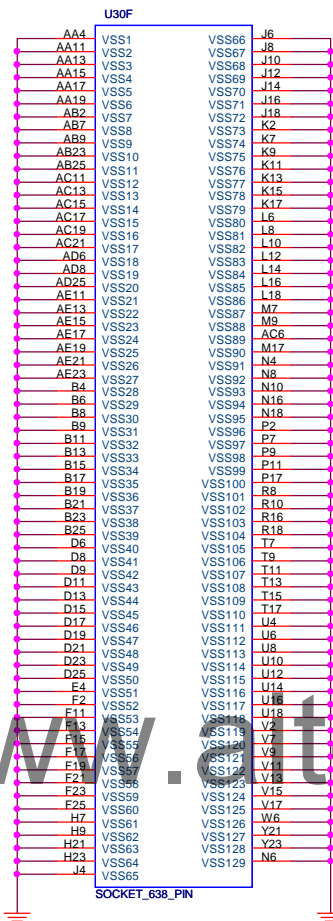
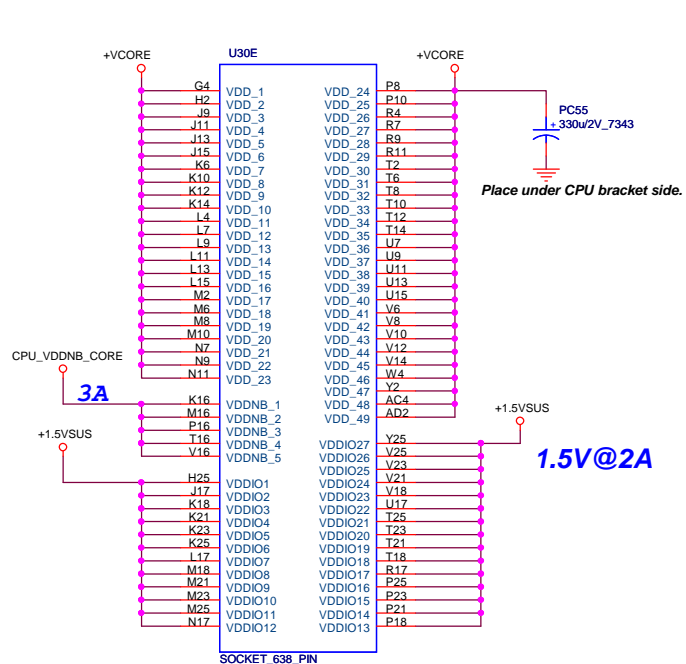




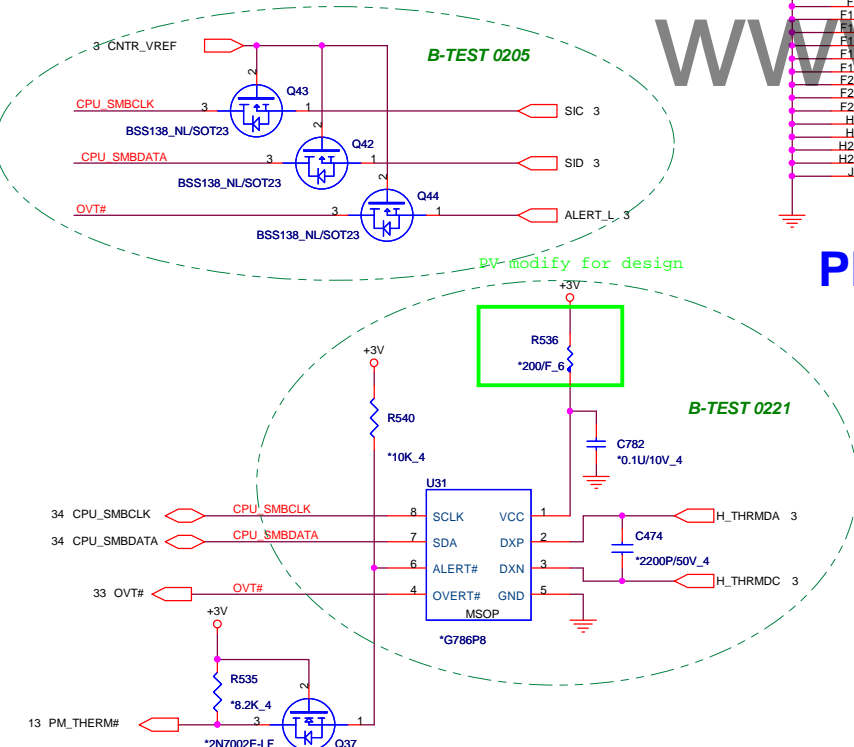






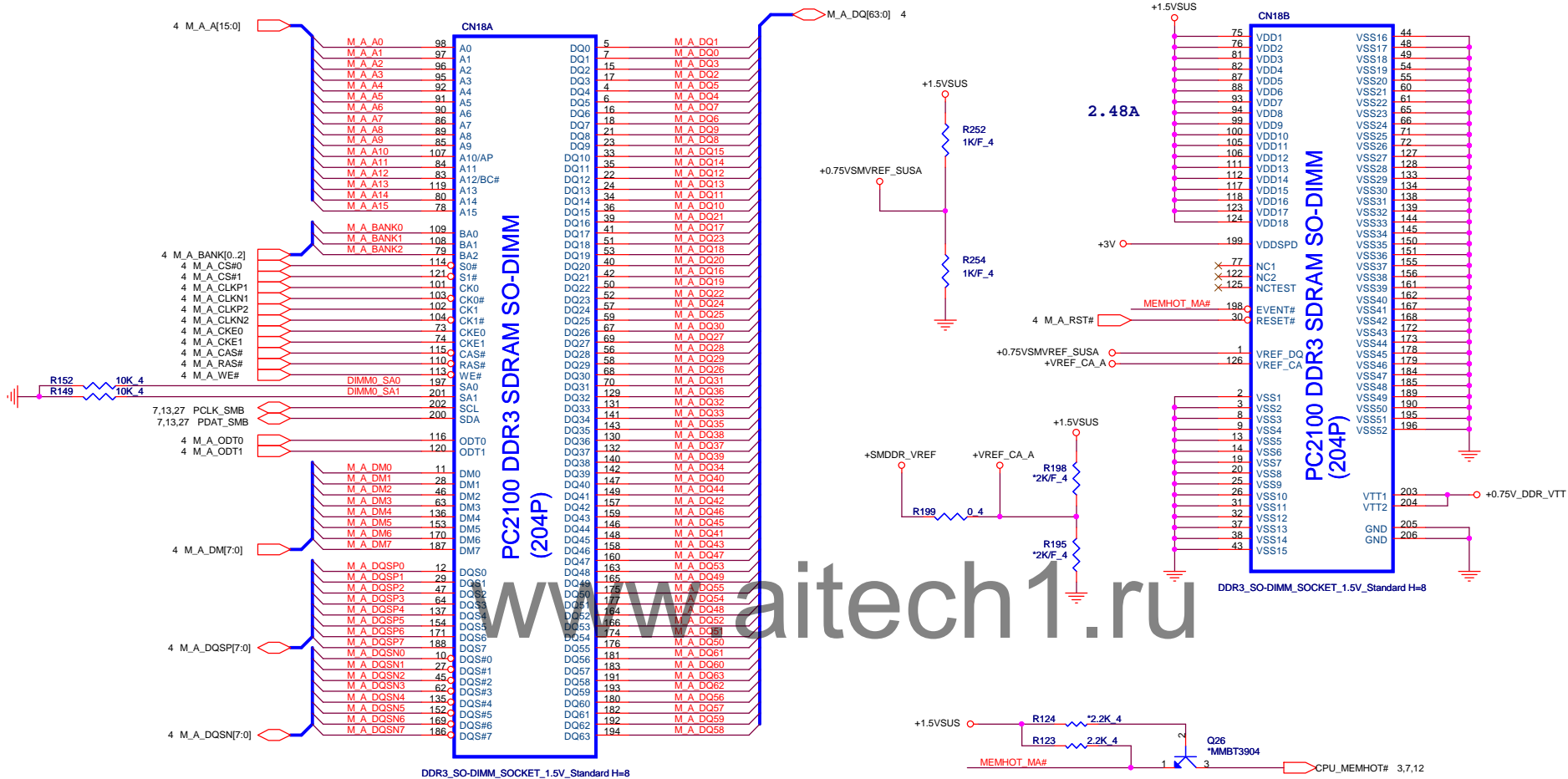


# PROCESSOR POWER AND GROUND

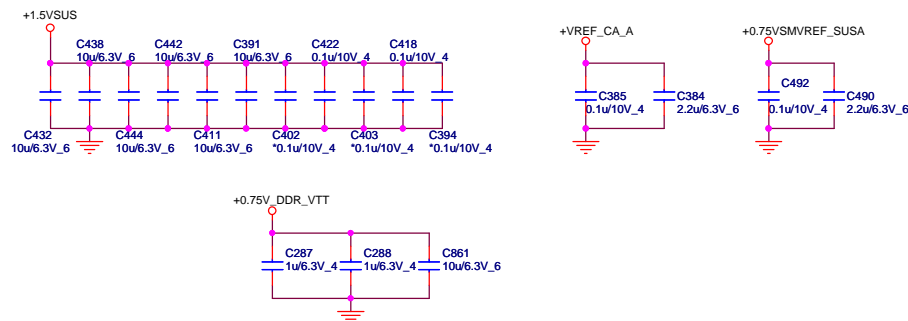


- 3,4,6,7,15,29,38,41,43,44 +1.5VSUS
- 38 CPU\_VDDNB\_CORE +V CORE
- 12,13,15,16,26,27,29,32,35,37 +3V\_S5
- 3,6,7,10,11,12,13,14,15,16,18,20,25,26,27,29,30,32,33,34,35,37,38,39,40,41,42,43,44 +3V





### Place these Caps near So-Dimm0.



3,4,5,7,10,11,12,13,14,15,16,18,20,25,26,27,29,30,32,33,34,35,37,38,39,40,41,42,43,44 +1.5VSUS  
 3,5,7,10,11,12,13,14,15,16,18,20,25,26,27,29,30,32,33,34,35,37,38,39,40,41,42,43,44 +3V  
 4,7,41 +0.75V\_DDR\_VTT



**Quanta Computer Inc.**

**PROJECT : ZRA**

**DDR3 DIMMA-STD**

Size Document Number

Date: Monday, March 29, 2010

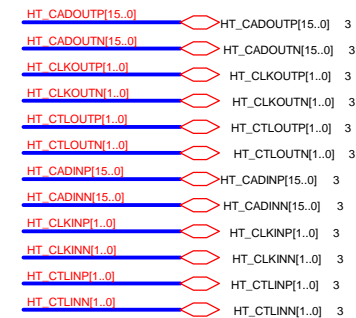
Sheet 6 of 48

Rev 1A







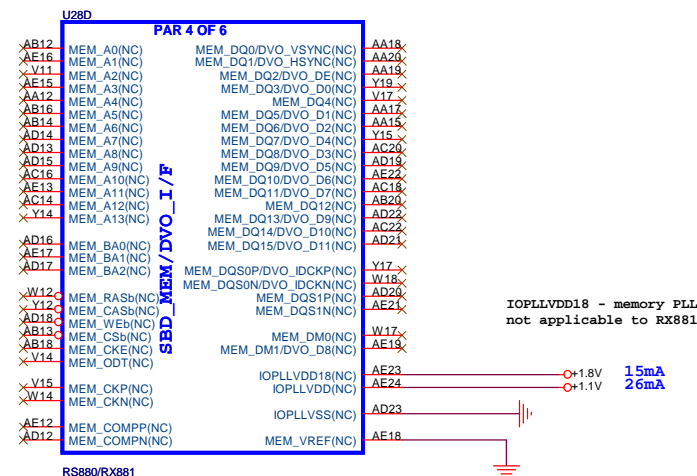


| signals   | RS880            | RX880              |
|-----------|------------------|--------------------|
| HT_TXCALP | Ra<br>301 ohm 1% | Ra<br>1.21k ohm 1% |
| HT_TXCALN |                  |                    |
| HT_RXCALP | Rb<br>301 ohm 1% | Rb<br>1.21k ohm 1% |
| HT_RXCALN |                  |                    |

RES CHIP 1.21K 1/16W +-1%(0402)  
 P/N : CS21212FB18

This block is for UMA only , Discrete can remove all component

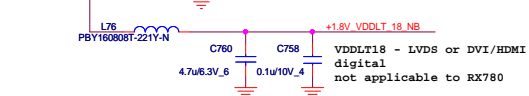
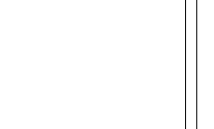
www.aitech1.ru








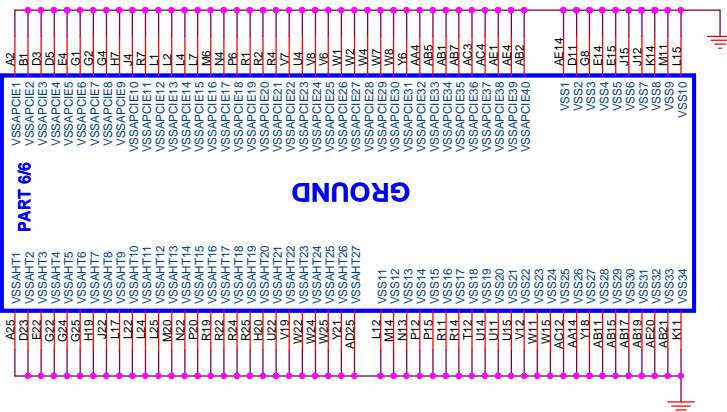


[illegible]

|   |                        |                |
|---|------------------------|----------------|
|  <b>Quanta Computer Inc.</b><br><b>PROJECT : ZRA</b> |                        | Rev<br>1A      |
| Size  | Document Number        |                |
| <b>RS880M-SYSTEM I/F 3/4</b>  |                        |                |
| Date:   | Monday, March 29, 2010 | Sheet 10 of 48 |



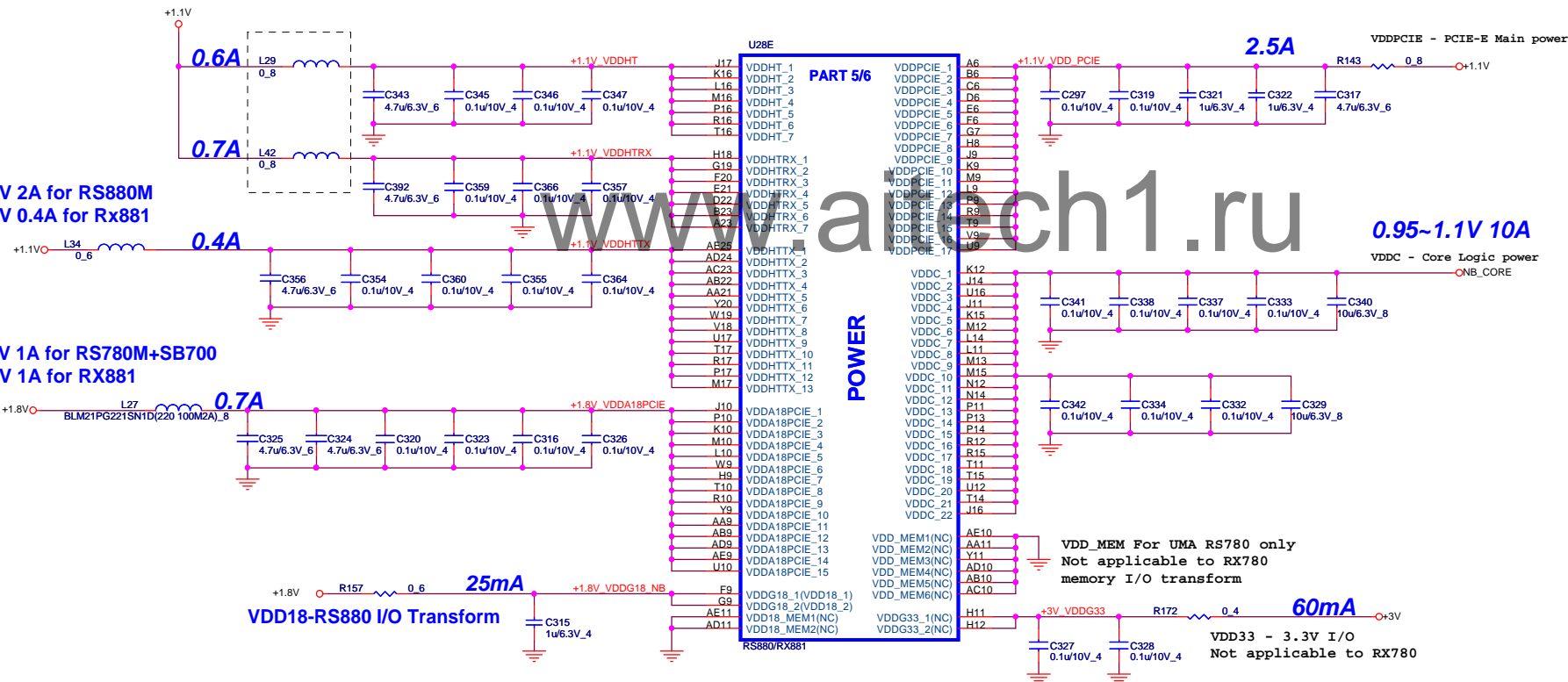
U28F



RX881/RS880 POWER DIFFERENCE TABLE

| PIN NAME   | RX881 | RS880      | PIN NAME      | RX881 | RS880 |
|------------|-------|------------|---------------|-------|-------|
| VDDHT      | +1.1V | +1.1V      | IOPLLVD       | +1.1V | +1.1V |
| VDDHTRX    | +1.1V | +1.1V      | AVDD          | GND   | +3.3V |
| VDDHTTX    | +1.2V | +1.2V      | AVDDI         | GND   | +1.8V |
| VDDA18PCIE | +1.8V | +1.8V      | AVDDQ         | GND   | +1.8V |
| VDDG18     | +1.8V | +1.8V      | PLLVD         | GND   | +1.1V |
| VDD18_MEM  | GND   | +1.8V      | PLLVD18       | GND   | +1.8V |
| VDDPCIE    | +1.1V | +1.1V      | VDDA18PCIEPLL | +1.8V | +1.8V |
| VDDC       | +1.1V | +1.1V      | VDDA18HTPLL   | +1.8V | +1.8V |
| VDD_MEM    | GND   | +1.8V/1.5V | VDDLTP18      | GND   | +1.8V |
| VDDG33     | +3.3V | +3.3V      | VDDLTP18      | GND   | +1.8V |
| IOPLLVD18  | +1.8V | +1.8V      | VDDLTP33      | NC    | NC    |

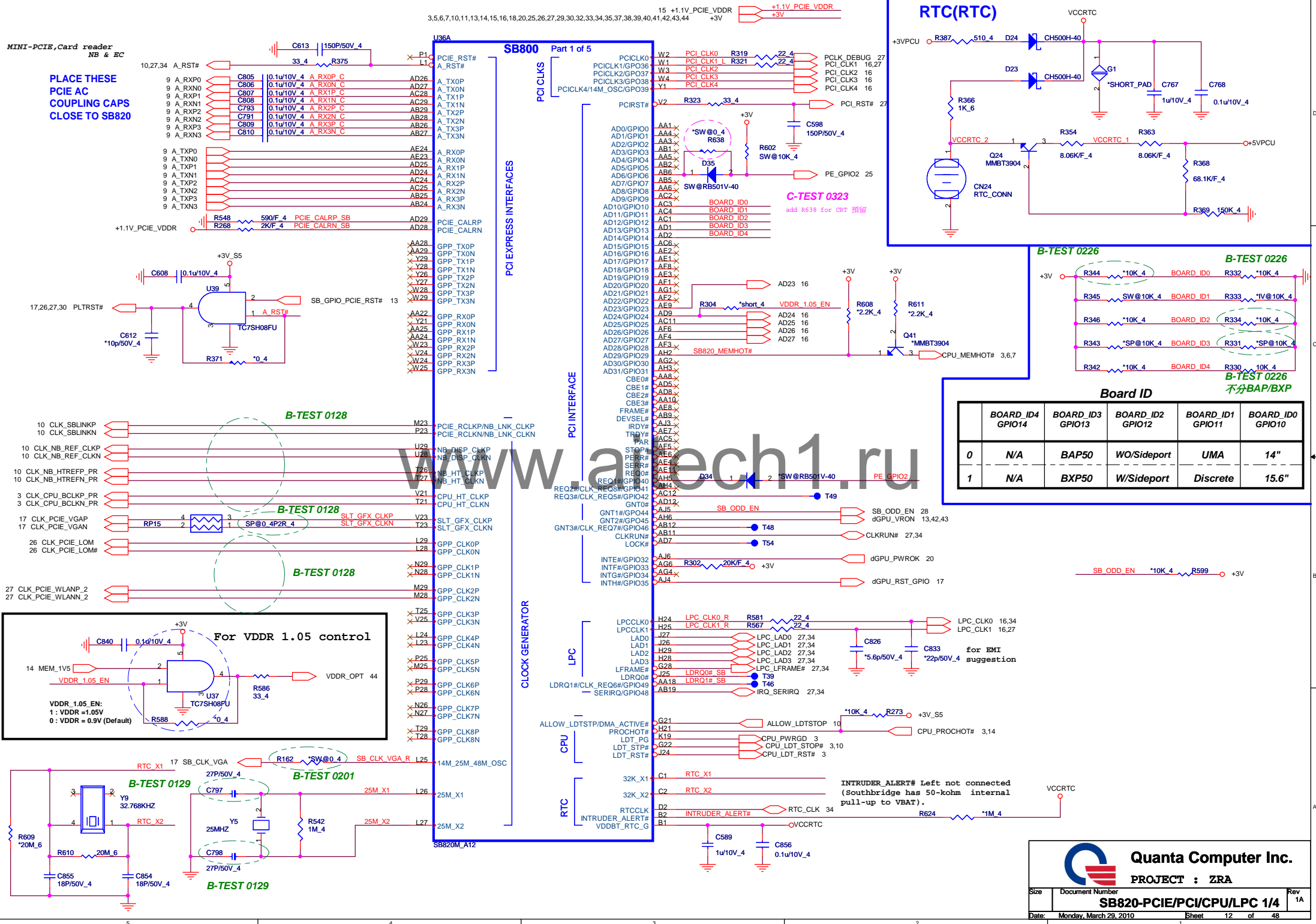
+1.1V 2A for RS880M  
+1.1V 1.3A for RX881



+1.1V 3,8,9,10,15,39  
+1.8V 8,10,16,25,38,43,44  
NB\_CORE 33,40



PLACE THESE  
PCIE AC  
COUPLING CAPS  
CLOSE TO SB820

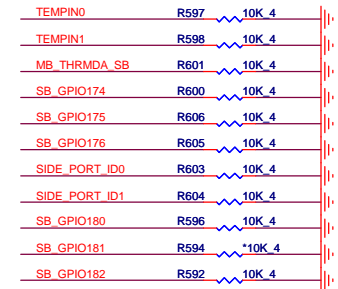






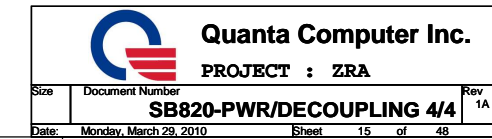


## SATA ODD





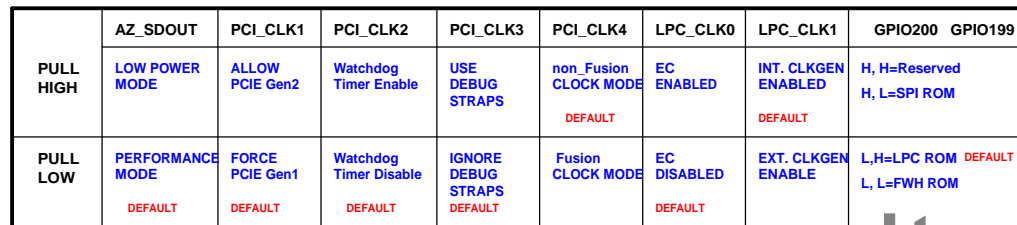
VDD-- S/B CORE power



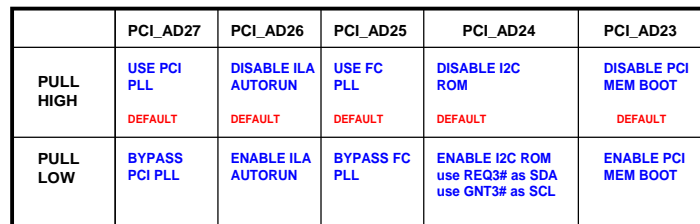


**POSSIBLE FOR DUAL-UP RESISTORS.**

For  
internal  
clock GEN.



SB800 HAS 15K INTERNAL PU FOR PCI\_AD[27:23]



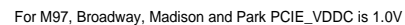
12,13,15,26,27,29,32,35,37 +3V\_S5  
8,10,11,25,38,43,44 +1.8V



SOT23-5



U24A



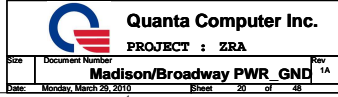










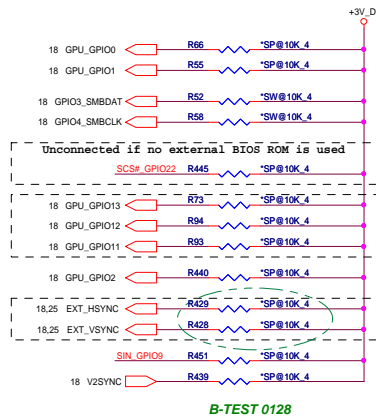








## PIN STRAPS



## Memory Aperture size

| GPIO[13:11] | Size  |
|-------------|-------|
| 000         | 128MB |
| 001         | 256MB |
| 010         | 64MB  |
| 011         | 32MB  |

## Function Table

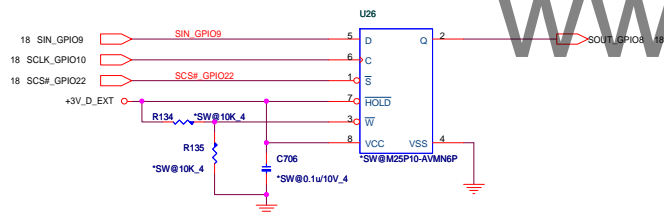
| EXT_HSYNC | EXT_VSYNC | Discription       |
|-----------|-----------|-------------------|
| 0         | 0         | No Audio          |
| 0         | 1         | Any one by detect |
| 1         | 0         | DP only           |
| 1         | 1         | Both DP & HDMI    |

## CONFIGURATION STRAPS

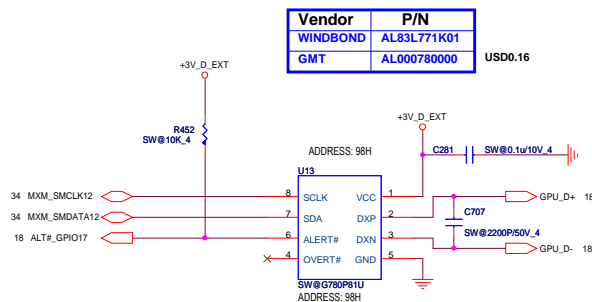
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

| STRAPS                                  | PIN                       | DESCRIPTION OF DEFAULT SETTINGS  | DEFAULT | REMARK   |
|---|---------------------------|--|---------|--|
| TX_PWRS_ENB                             | GPIO0                     | 0 = 50% TX OUTPUT SWING<br>1 = FULL TX OUTPUT SWING  | 0       |  |
| TX_DEEMPH_EN                            | GPIO1                     | 0 = POE TRANSMITTER DE-EMPHASIS ENABLED<br>1 = TX DE-EMPHASIS DISABLED<br>0 = TX DE-EMPHASIS ENABLED<br>1 = TX DE-EMPHASIS DISABLED<br>ENABLE EXTERNAL BIOS ROM<br>0 = DISABLE<br>1 = ENABLE | 0       |  |
| BIOS_ROM_EN                             | GPIO_22_ROMCSB            |  | 0       |  |
| ROMIDCFG(2:0)                           | GPIO[13:11]               | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT<br>NUMONYX_M25P10A:101  | 000     | See ROM table  |
| BIF_GEN2_EN_A                           | GPIO2                     | 0 = PCIE DEVICE AS 2.5GT/S CAPABLE<br>1 = PCIE DEVICE AS 5GT/S CAPABLE   | 0       | (Recommended setting as 5.0 GT/s capability will be controlled by software.) |
| GPIO_8_ROMSO<br>H2SYNC<br>GPIO_21_BB_EN | GPIO8<br>H2SYNC<br>GPIO21 | Reserved Only  | 0       |  |
| AUD[1:0]                                | HSYNC<br>VSYNC            | AUD[1:0]<br>00: NO AUDIO FUNCTION.<br>01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED.<br>10: AUDIO FOR DISPLAYPORT ONLY.<br>11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.              | 11      | See Audio table  |
| GPIO_9_ROMSI                            | GPIO9                     | 0 = VGA controller capacity enable<br>1 = VGA controller capacity disable<br>(The device will not be recognized as the system's VGA controller.)   | 0       |  |
| VIP_DEVICE_STRAP_DIS                    | V2SYNC                    | 0 = DRIVER would ignore the value sample on VHAD_0 during RESET.<br>1 = DRIVER would use the value sample on VHAD_0 during RESET.  | 0       |  |

## SERIAL ROM Default don't put



## Thermal Sensor



## DDR3 Memory Aperture size

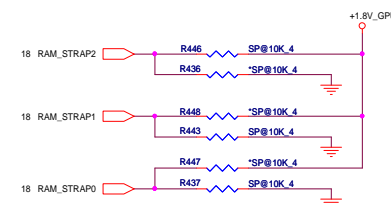
## DDR3 Memory Aperture size

| Vendor  | Vendor P/N      | STN B/S P/N             | Size  | RAM_STRAP2<br>DVDPDATA_2 | RAM_STRAP1<br>DVDPDATA_1 | RAM_STRAP0<br>DVDPDATA_0 |
|---------|-----------------|-------------------------|-------|--------------------------|--------------------------|--------------------------|
| Hynix   | H5TQ1G63BFR-12C | AKD5LZGTW04<br>(64M*16) | 512Mb |                          |                          |                          |
|         |                 |                         | 1Gb   | 1                        | 0                        | 0                        |
|         |                 |                         | 2Gb   |                          |                          |                          |
| Samsung | K4W1G1646E-HC12 | AKD5LGGT506<br>(64M*16) | 512Mb |                          |                          |                          |
|         |                 |                         | 1Gb   | 0                        | 0                        | 0                        |
|         | K4W2G1646B-HC12 | AKD5MGGT500             | 2Gb   |                          |                          |                          |
| AMD     | 23EY2387MA12-SZ | AKD5LGGT700             | 1Gb   | 0                        | 1                        | 0                        |

B-TEST 0128

+1.8V\_GPU +1.8V\_GPU 18,20,21,43

+3V\_D +3V\_D 17,18,20,25,35



RAM\_STRAP2 SET DDR3 Vendor

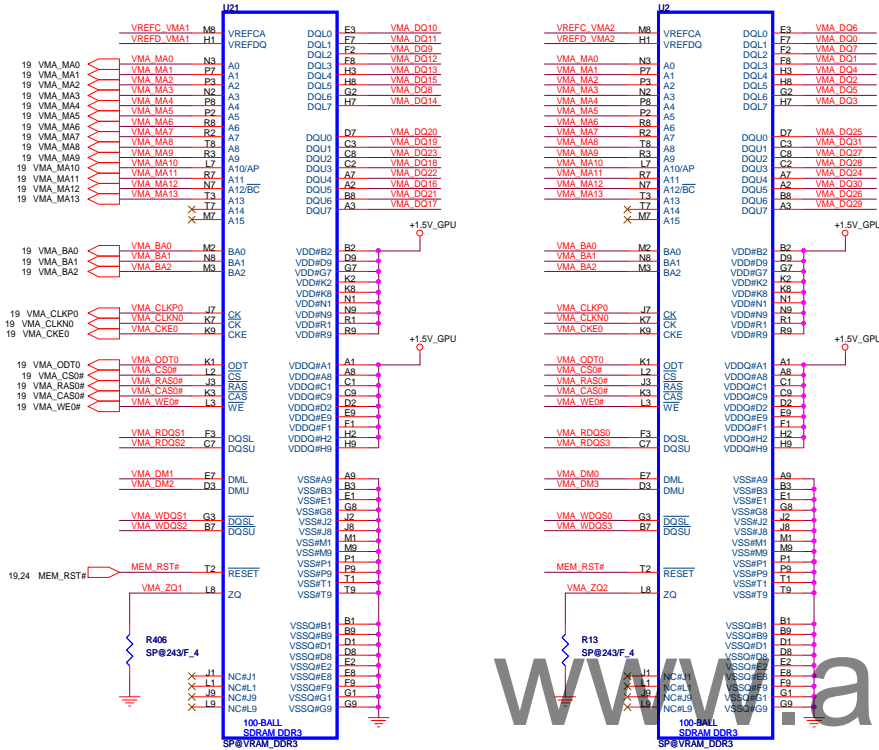
RAM\_STRAP[1:0] SET SIZE.



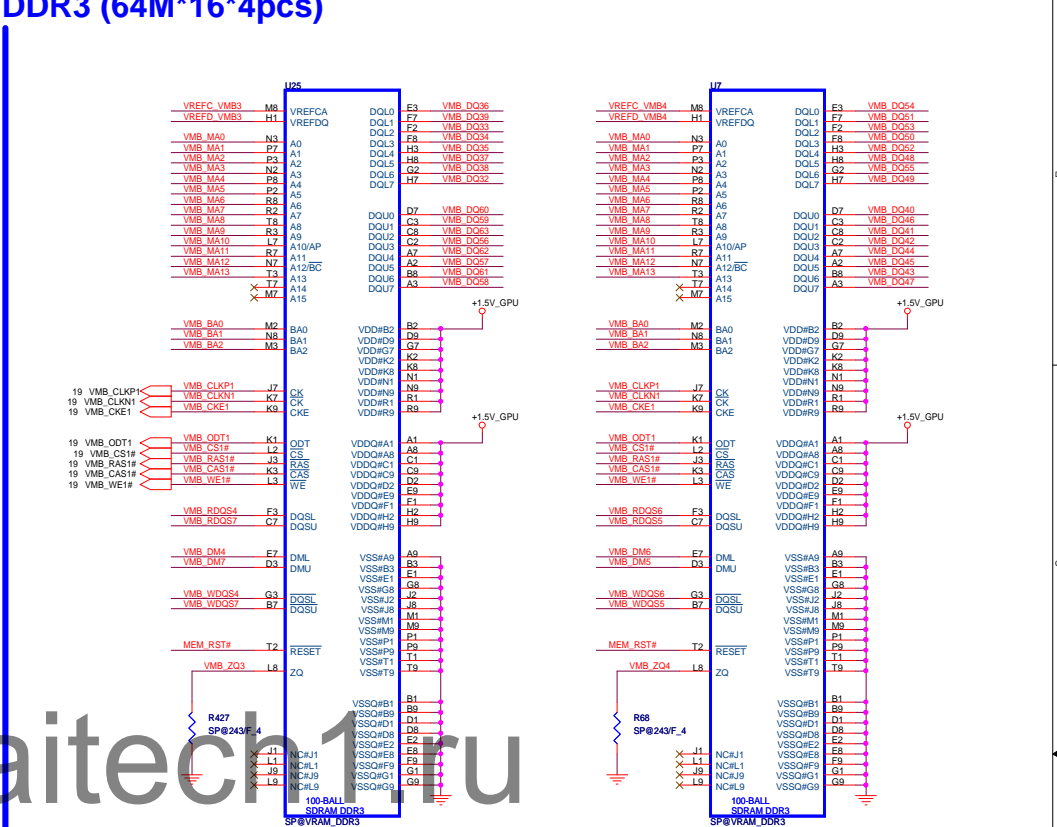
Park, M29M Use Channel B Memory Interface Only

# CHANNEL A: 512MB DDR3 (64M\*16\*4pcs)

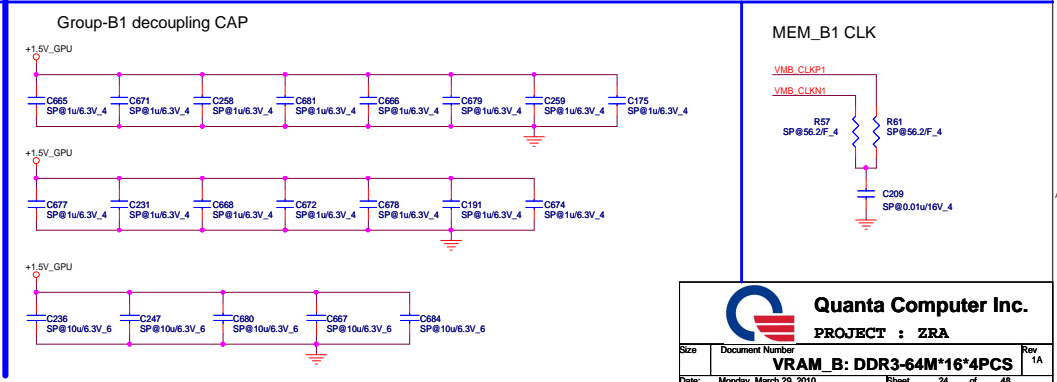
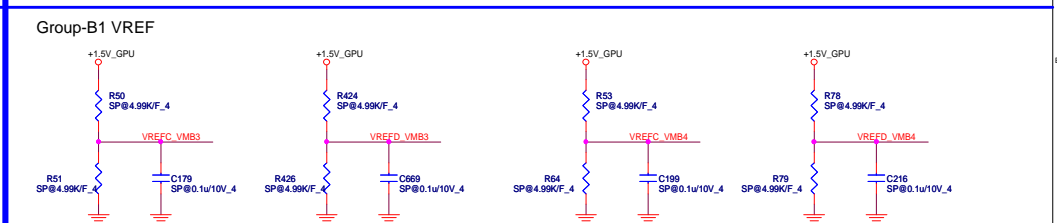
19 VMA\_DQ[63..0] VMA DQ[63..0]  
19 VMA\_DM[7..0] VMA DM[7..0]  
19 VMA\_RDQS[7..0] VMA RDQS[7..0] QSA[7..0]  
19 VMA\_WDQS[7..0] VMA WDQS[7..0] QSA#[7..0]







BOT Up

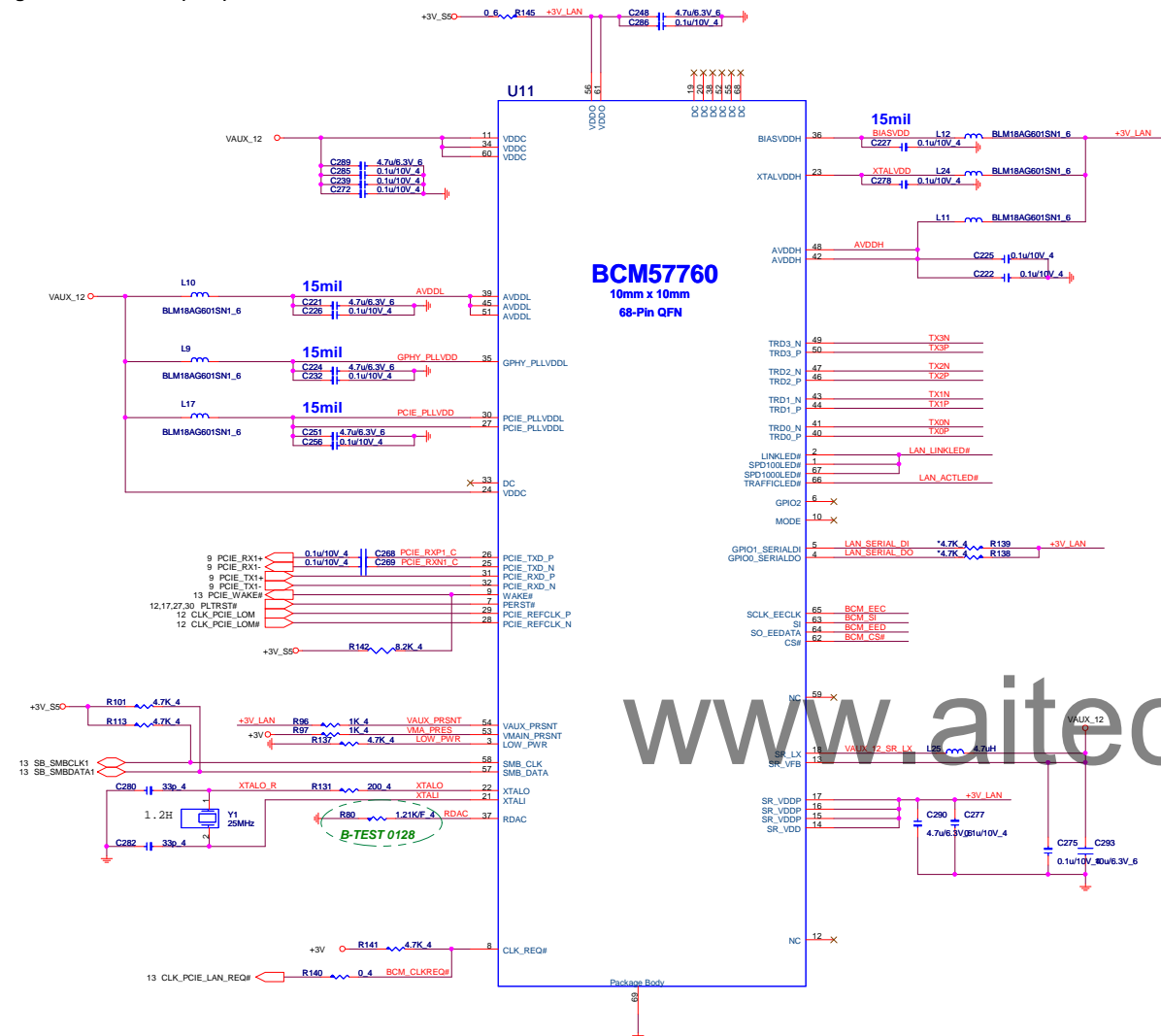




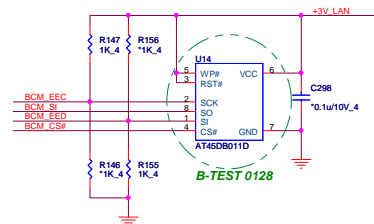




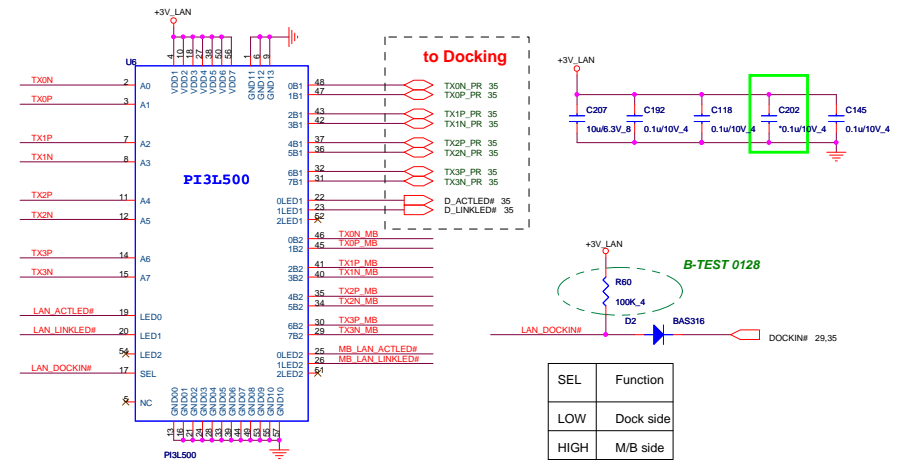
### Giga-LAN BCM57760(LAN)



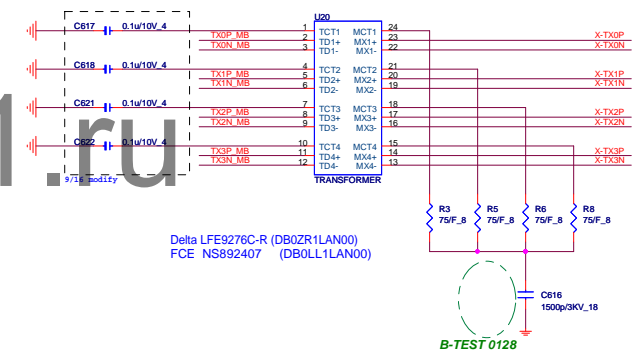
## Flash (1M) for ASF2.0



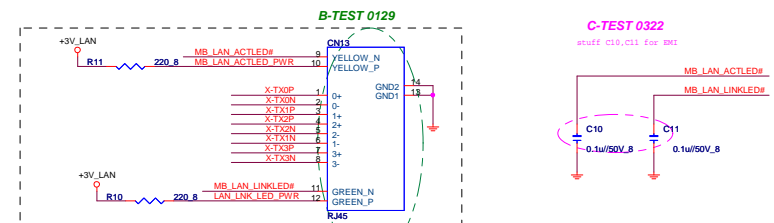
## LAN SWITCH



## TRANSFORMER



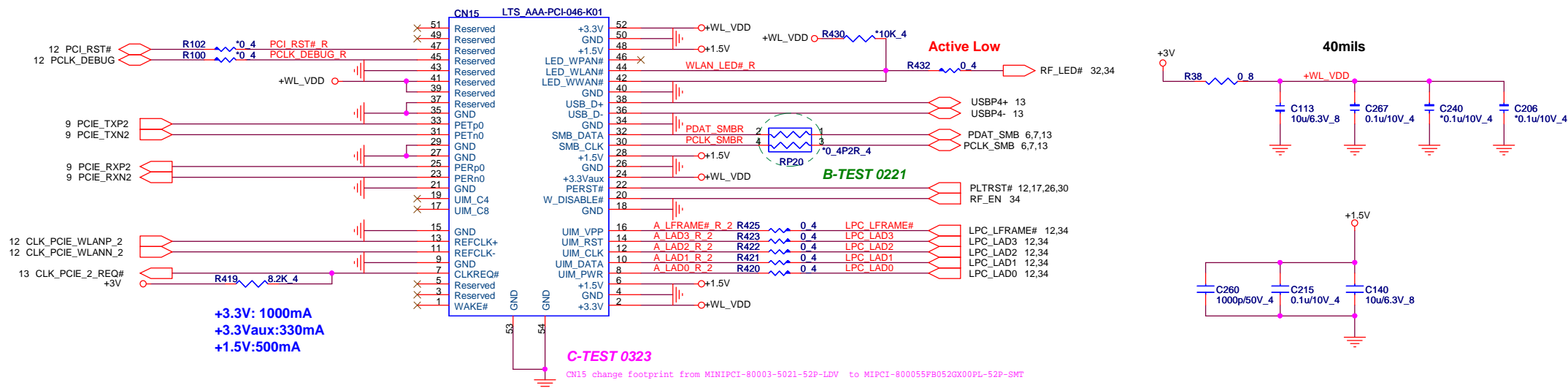
## RJ45(LAN)





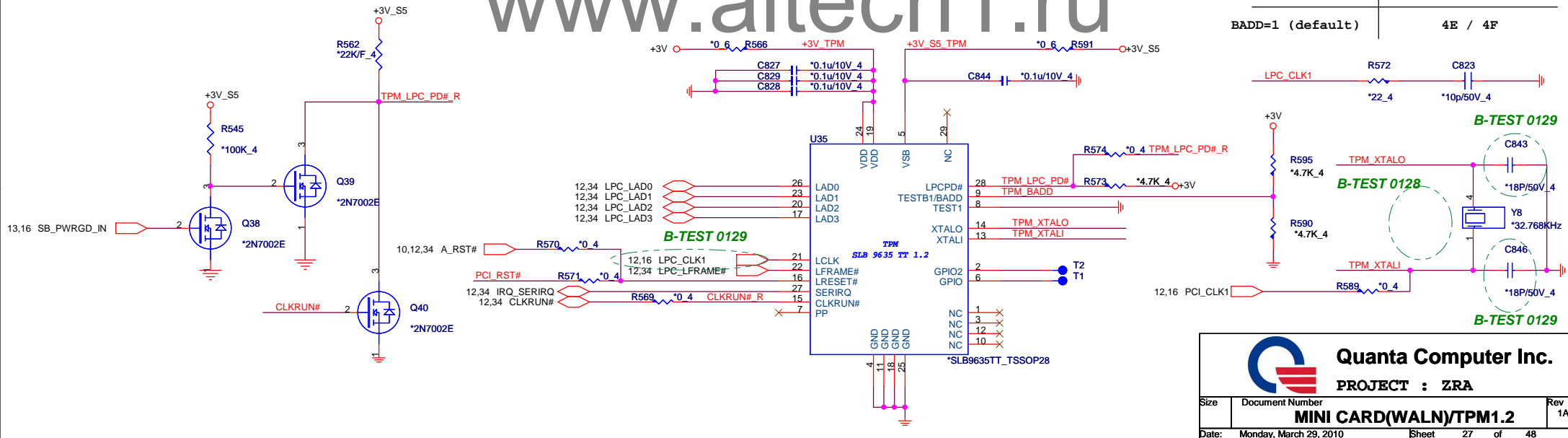
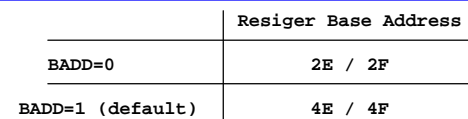
## MINI-CARD WLAN(MPC)

**H=7mm**



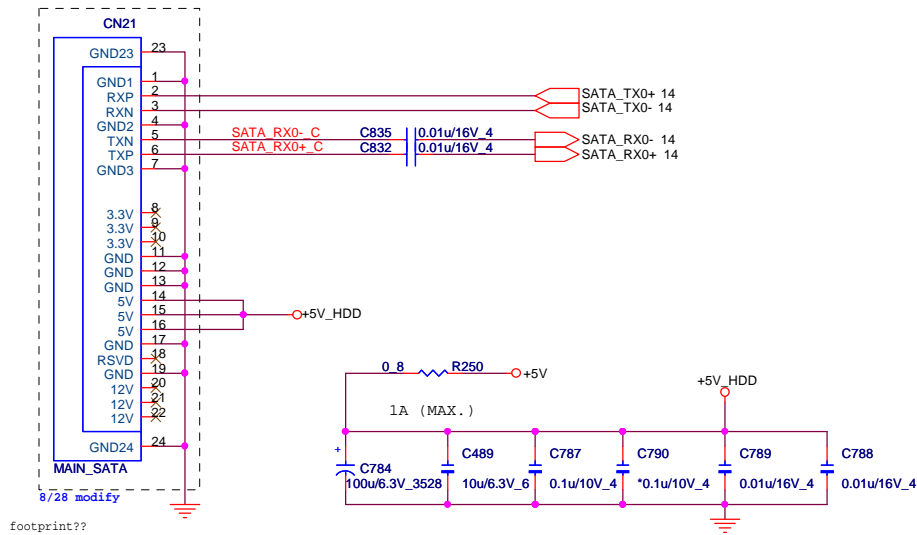
# TPM

[www.aitech1.ru](http://www.aitech1.ru)



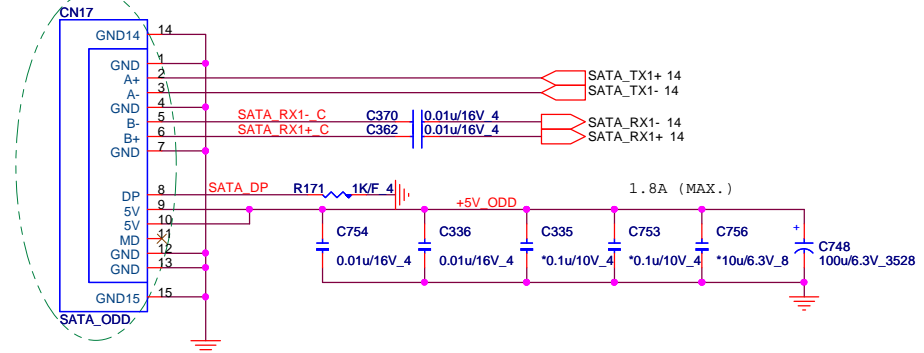


## SATA HDD(HDD)



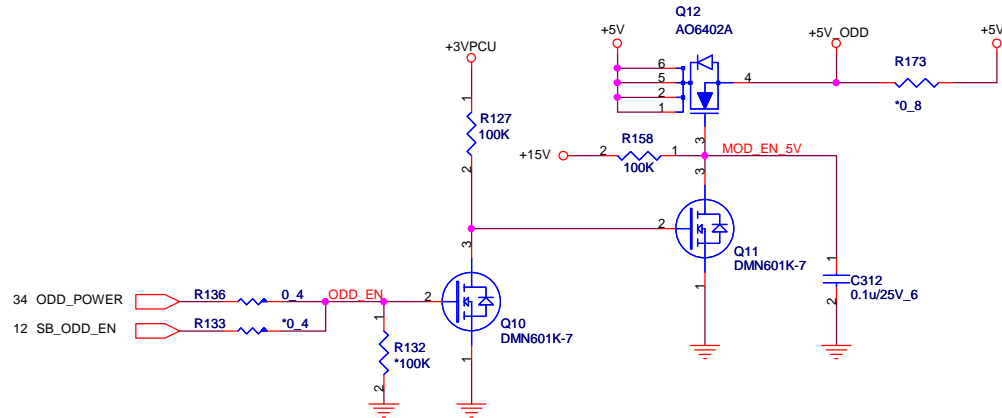
## SATA ODD (ODD)

B-TEST 0129



## ODD POWER(ODD)

www.aitech1.ru



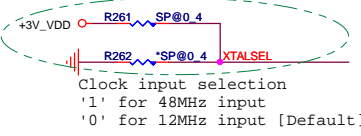




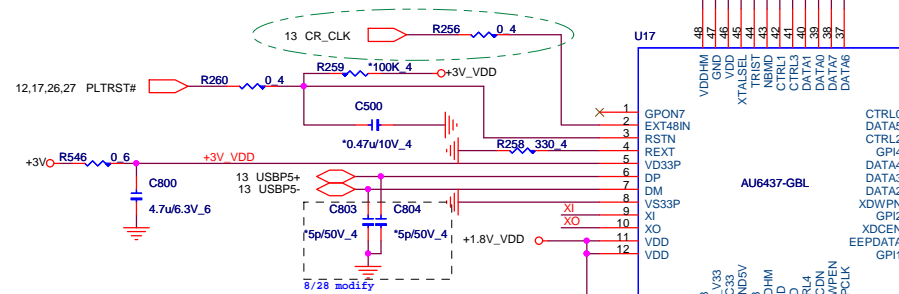


CARD READER (AU6437)

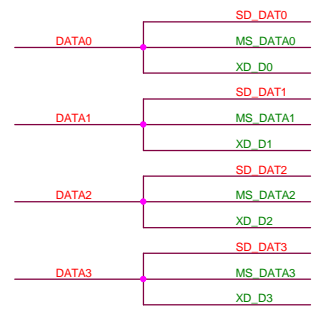
B-TEST 0223  
CLK source change from exterior to SB



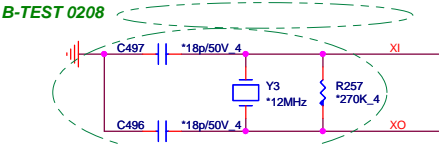
B-TEST 0208



CTRL0, CTRL1 trace length shorter, and surround with GND.



crystal trace width needs at least 10 mils.



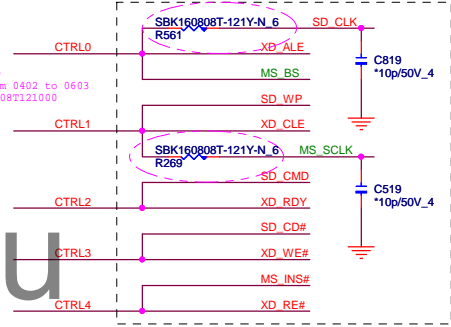
B-TEST 0223  
CLK source change from exterior to SB

pin13 output 20mils  
CAP close PIN11,12

SD write protect  
1:decided by SDWP[Default]  
0:letting SD always  
write-able

C-TEST 0322  
change R561,R269 footprint from 0402 to 0603  
and P/N from C800002J838 to CX08T121000  
FOR BM1

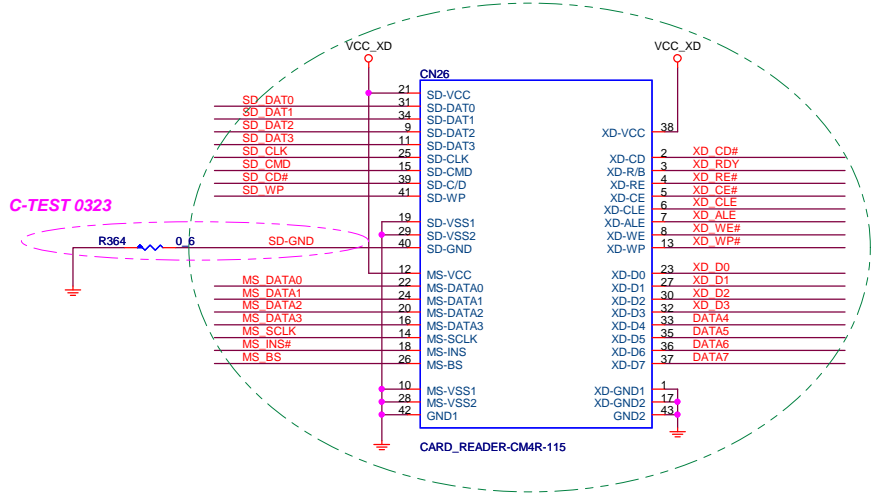
Close to connector



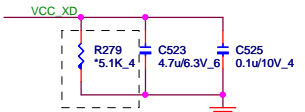
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4 IN 1 CARD READER (MMC)


B-TEST 0128



C-TEST 0323



Close to CN14 pin 14 & pin23  
4.7u CAP close to pin23



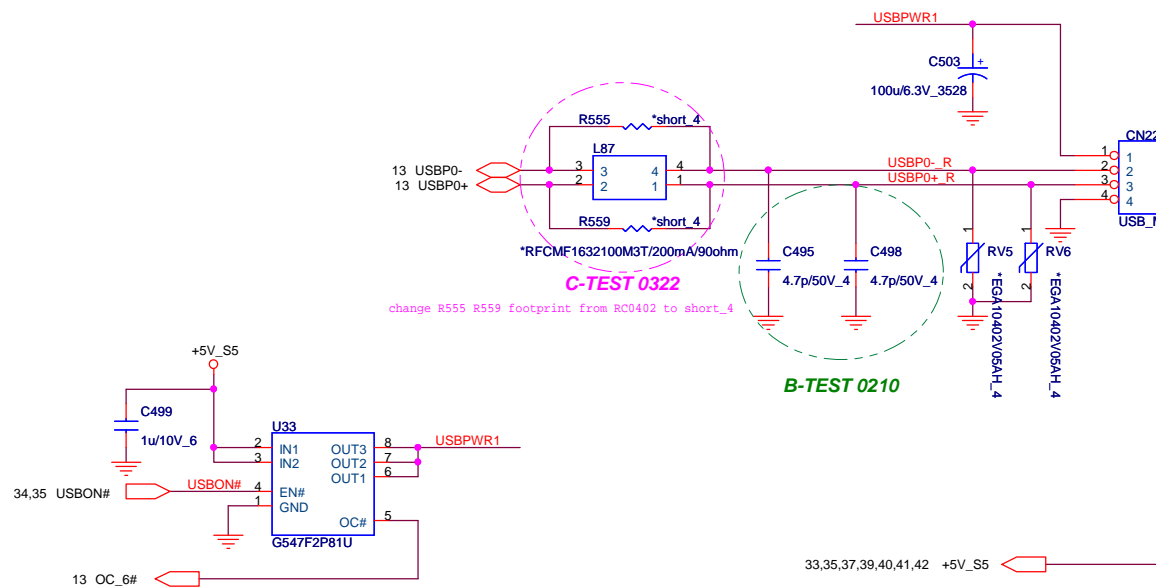
**Quanta Computer Inc.**

**PROJECT : ZRA**

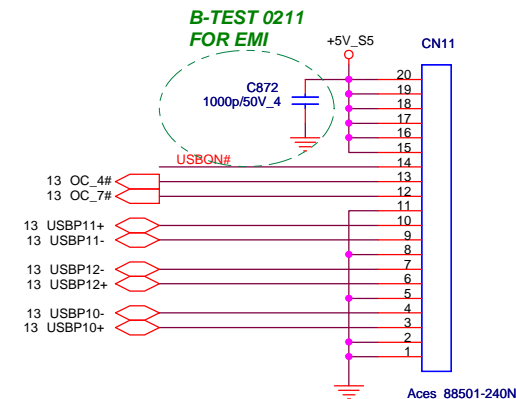
|       |                          |                |
|-------|--------------------------|----------------|
| Size  | Document Number          | Rev            |
|       | <b>CardReader AU6437</b> | 1A             |
| Date: | Monday, March 29, 2010   | Sheet 30 of 48 |



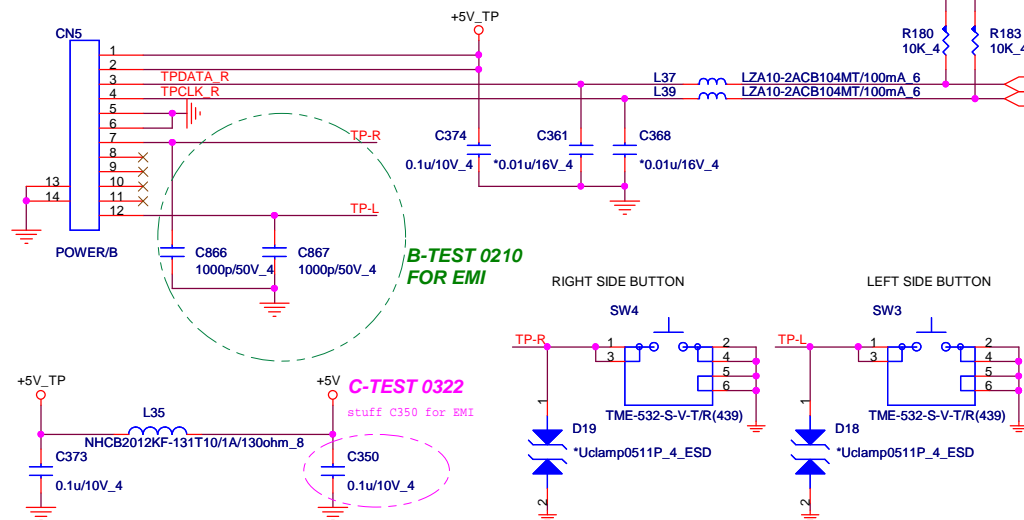
## USB PORT(USB)



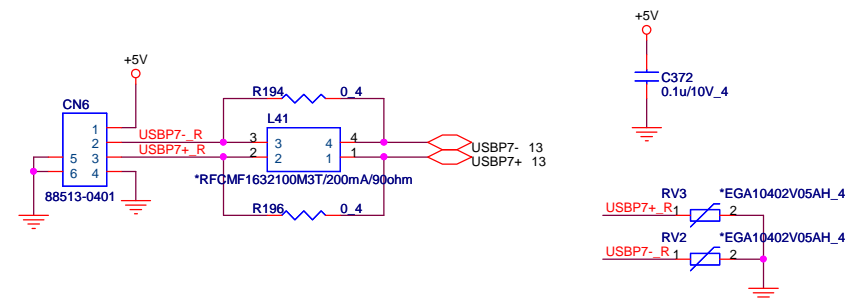
## USB BOARD CONN(USB)



## Touch Pad



## Finger Print

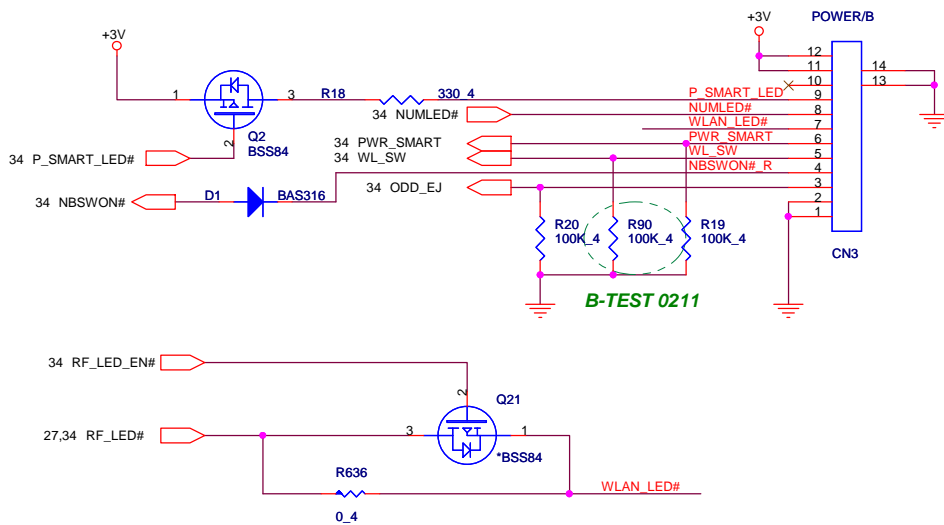


Quanta Computer Inc.  
PROJECT : ZRA

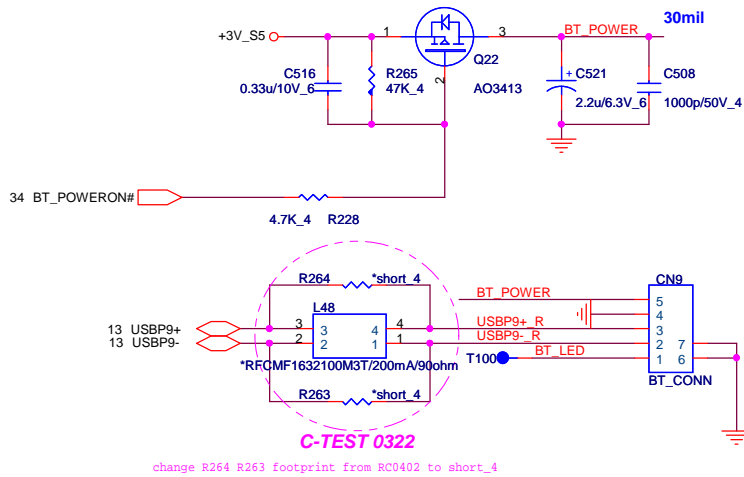
| Size  | Document Number        | Rev            |
|-------|------------------------|----------------|
|       | USB/USB DB/TP/FP       | 1A             |
| Date: | Monday, March 29, 2010 | Sheet 31 of 48 |



## POWER DB CONN(UIF)



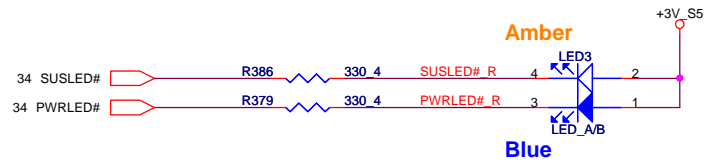
## BLUETOOTH CONN(BTM)



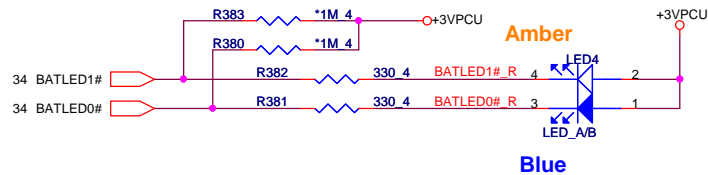
change R264 R263 footprint from RC9402 to short\_4

## LED(UIF)

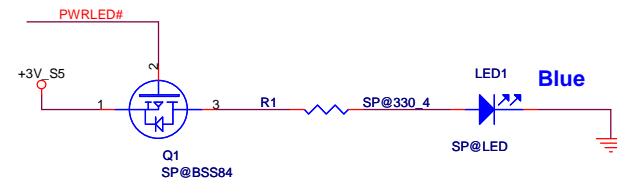
### Power LED



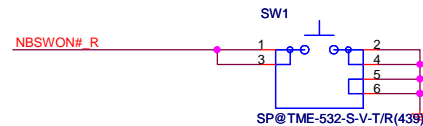
### Battery LED



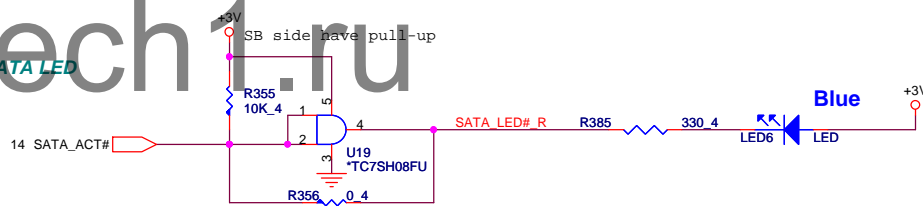
### BXP Power LED



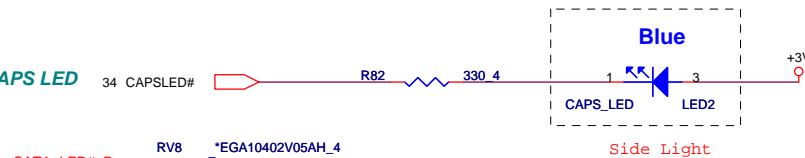
### BXP Power SW



### SATA LED



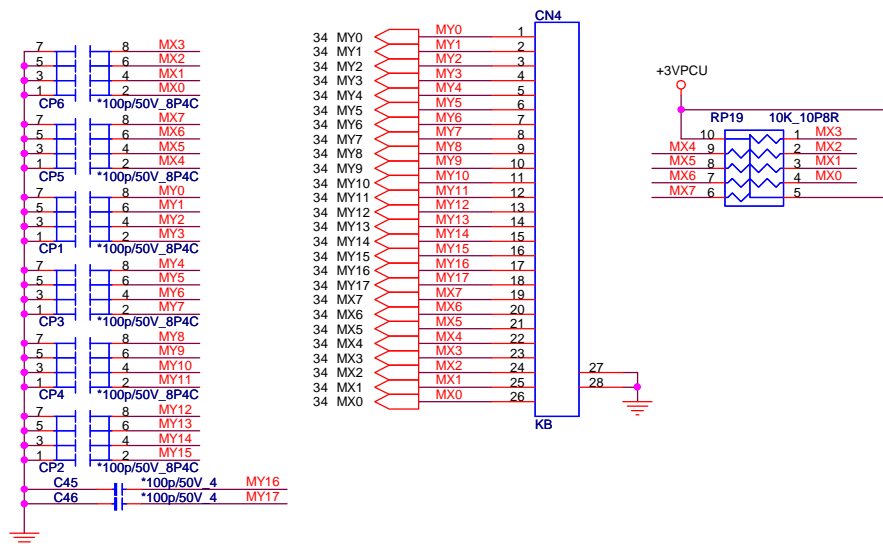
### CAPS LED



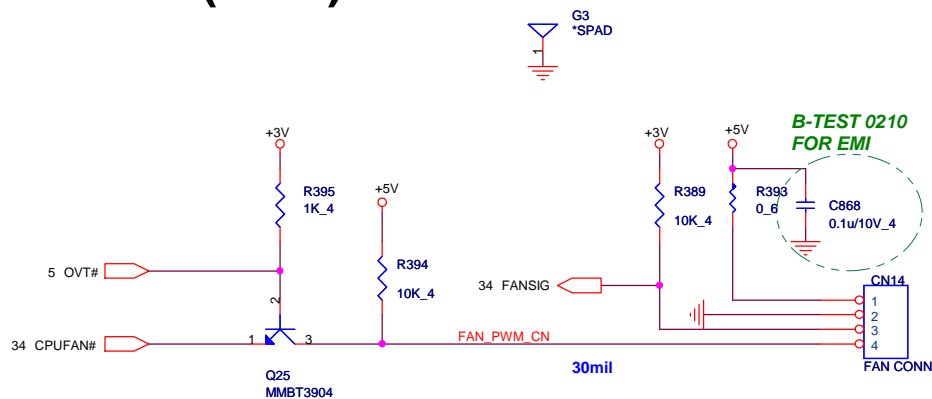
ESD(EMC)



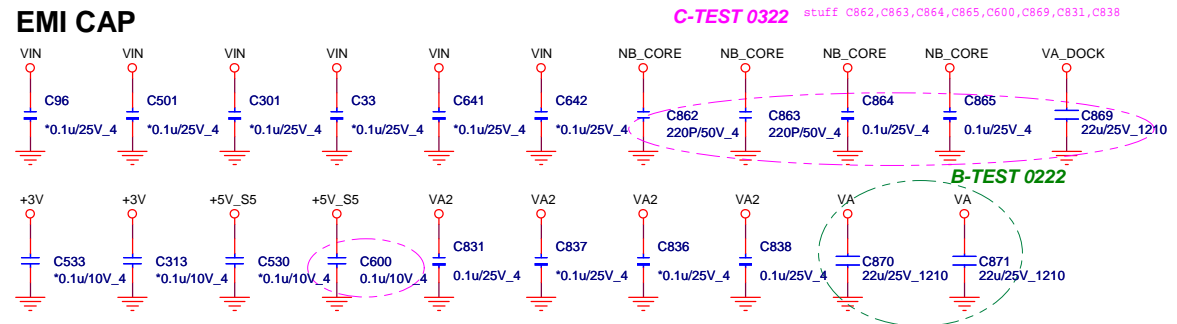
**K/B(KBC)**



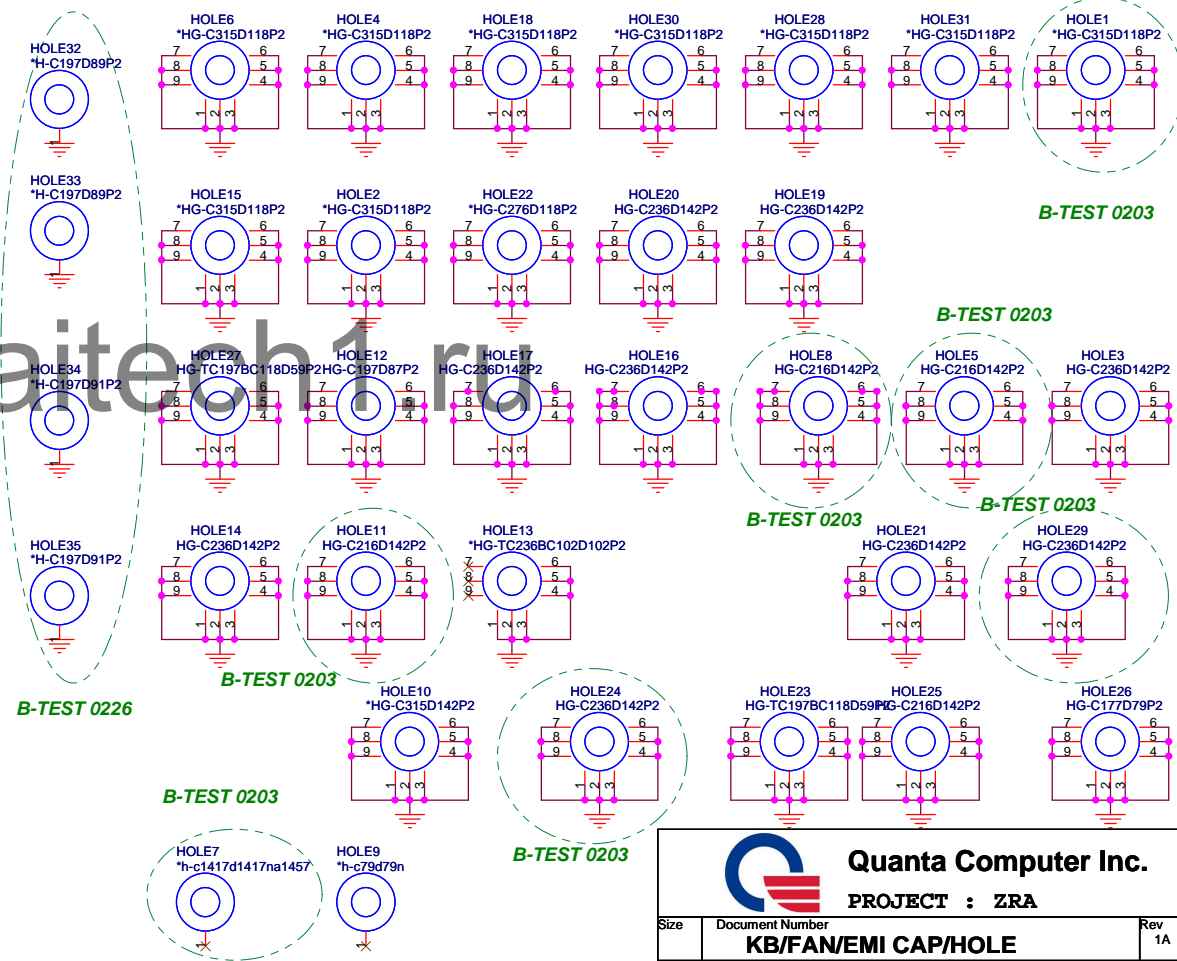
## CPU FAN(THM)



## EMI CAP



## HOLE(OTH)

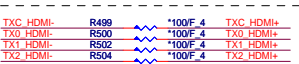








## DOCKING

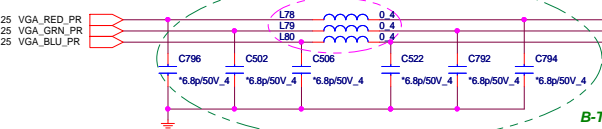


EMI

change L78 L79 L80 footprint from RC0603 to RC0402

**B-TEST 0210  
FOR EMI**

~~C-TEST 0324~~



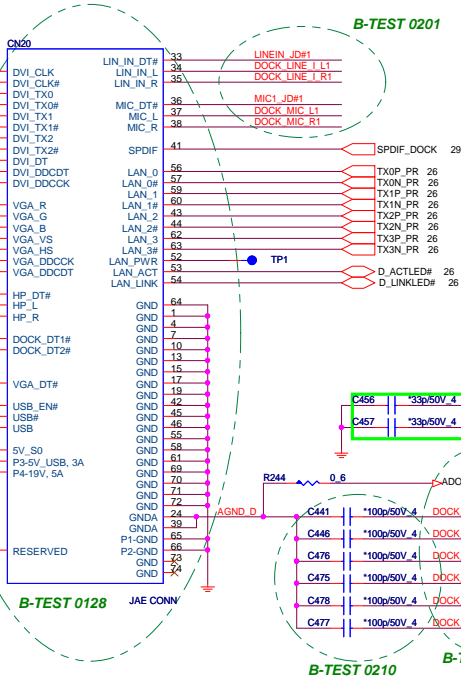
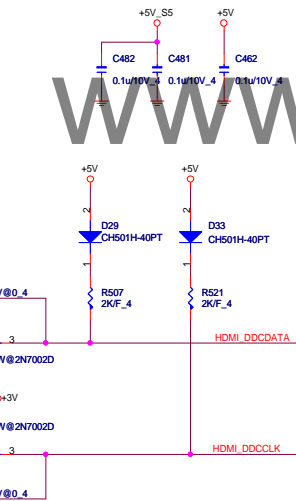
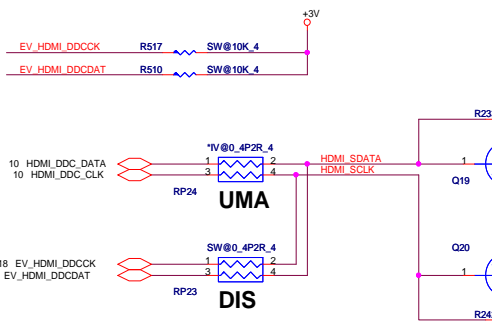
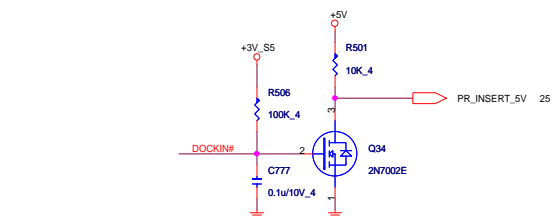
**B-TEST 0201**

Connect to EC.

D9 change footprint from SBM1040-3P to POWER-6 5-1 84-3P

**C-TEST 0323**

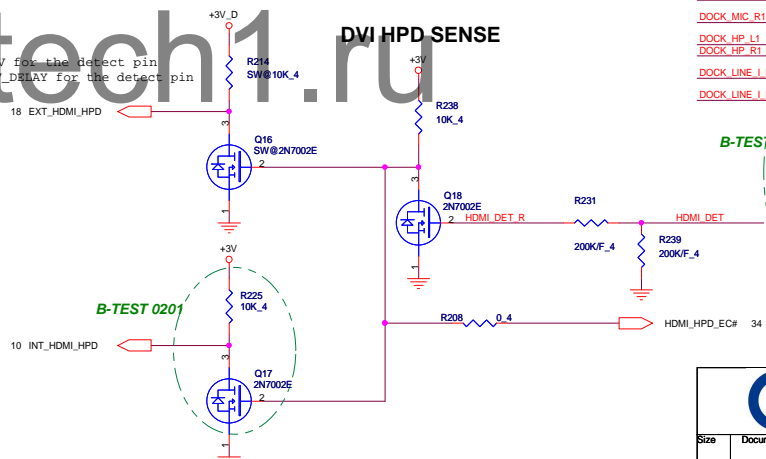
**B-TEST 0222**



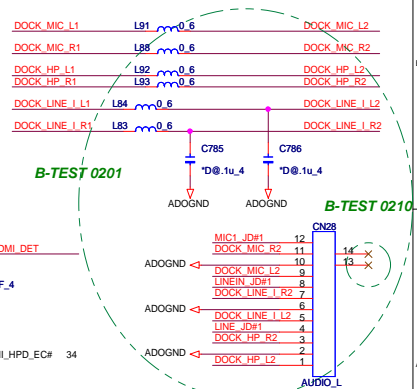
**B-TEST 0210**

**B-TEST 0201**

**DVI HPD SENSE**



**B-TEST 0201**



**B-TEST 0201**

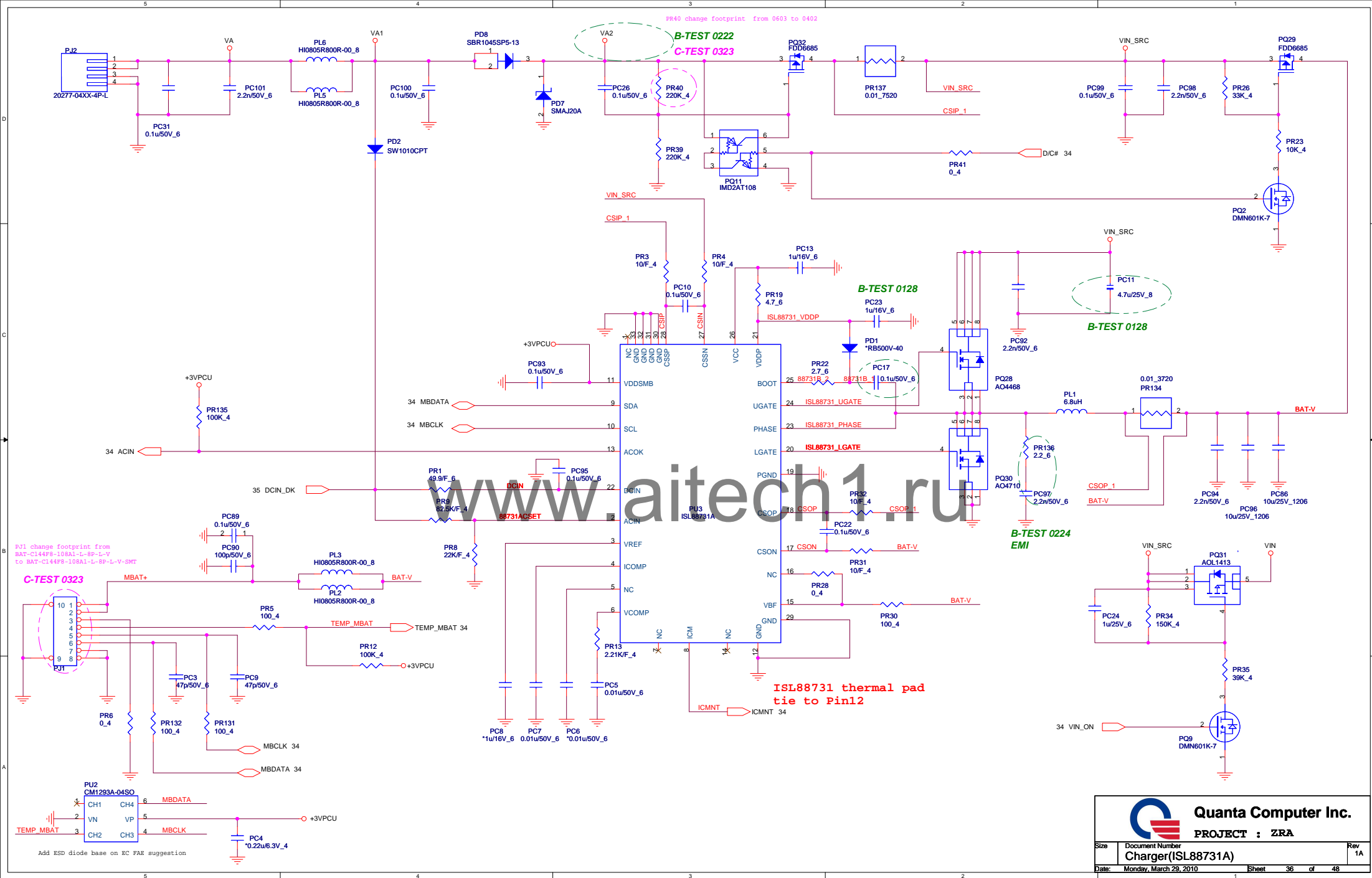
**B-TEST 0210**

**Quanta Computer Inc.**

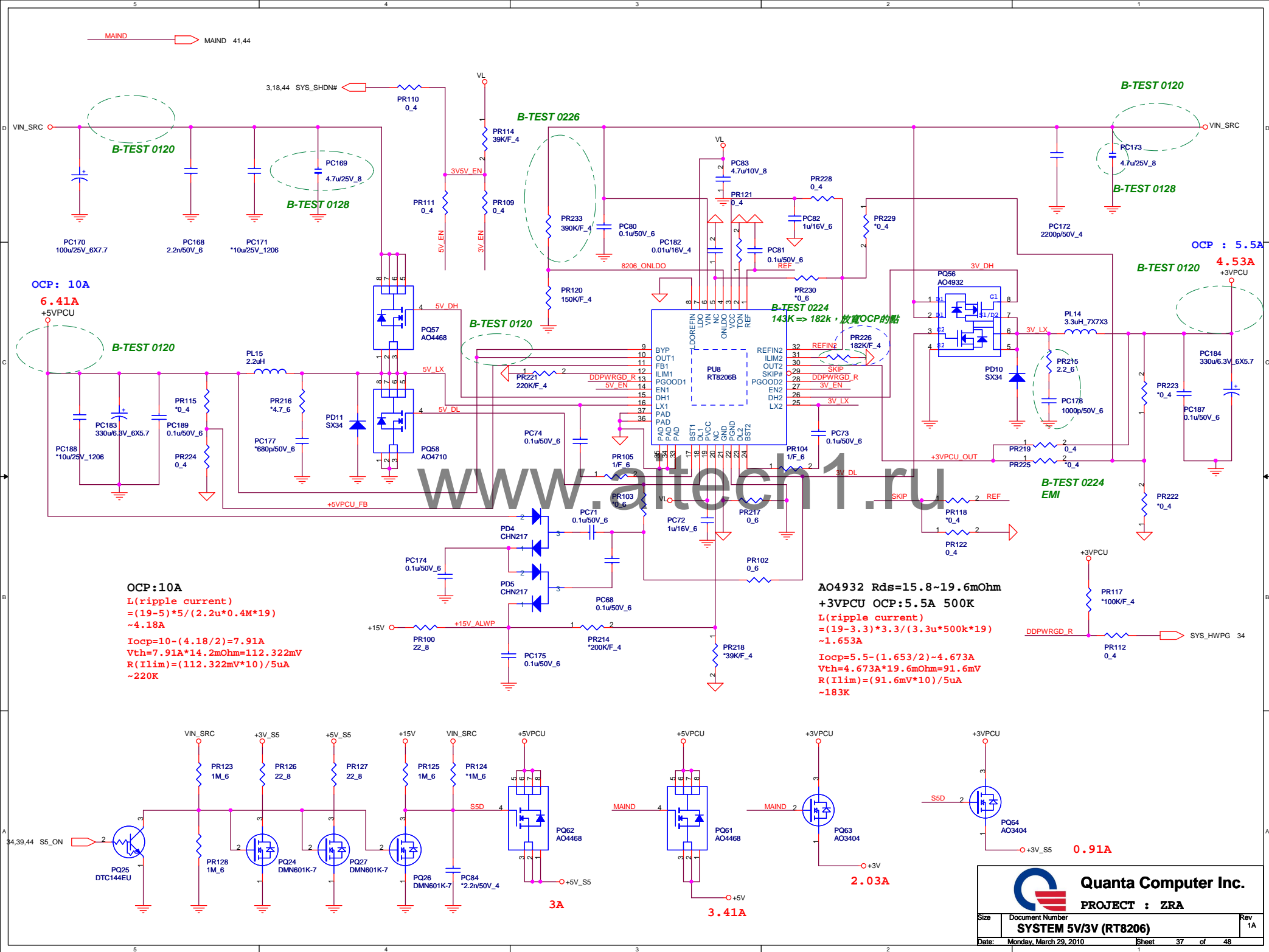
PROJECT : ZRA

|       |                        |                |
|-------|------------------------|----------------|
| Size  | Document Number        | Rev            |
|       | <b>Docking</b>         | 1A             |
| Date: | Monday, March 29, 2010 | Sheet 35 of 48 |



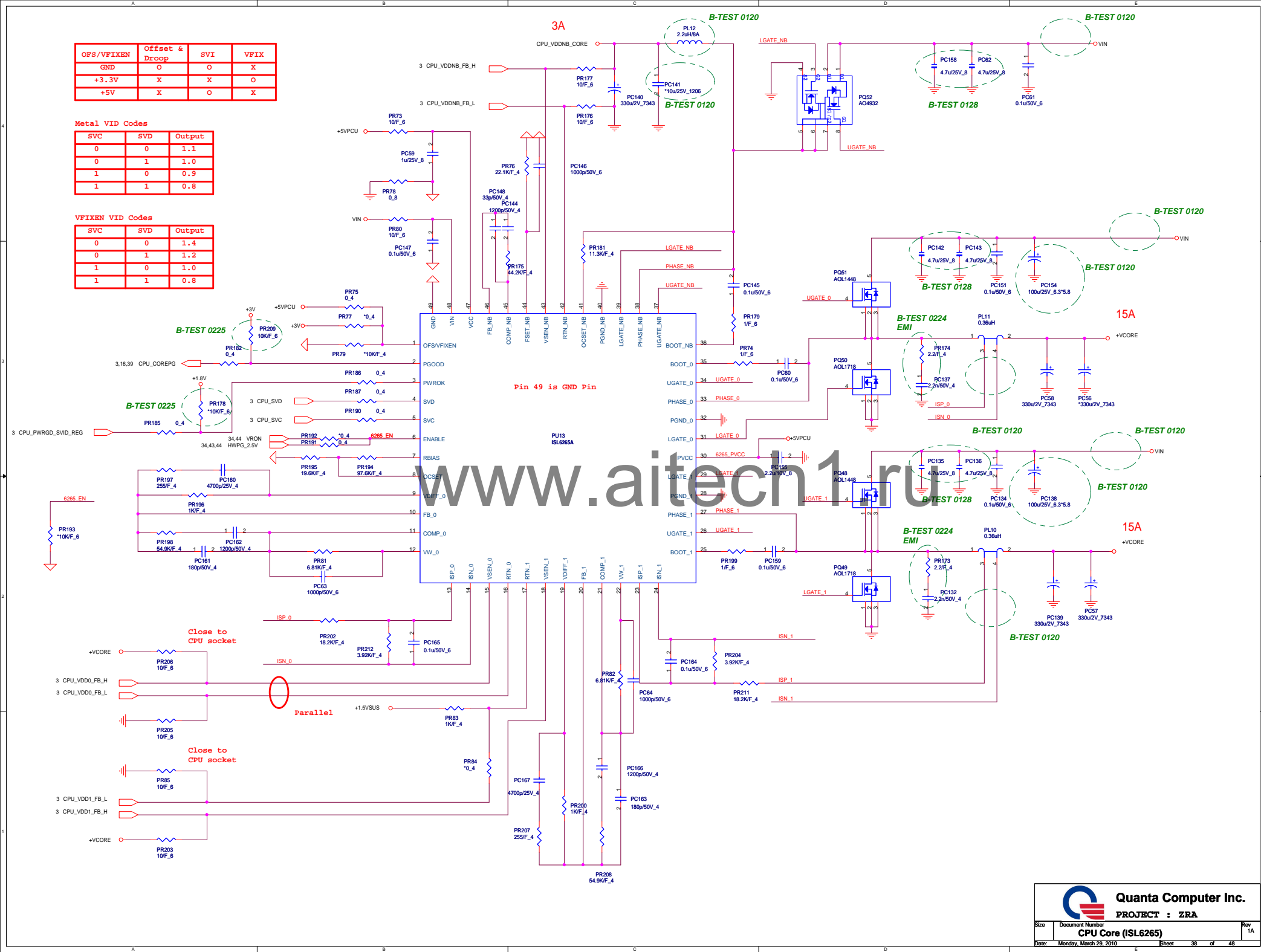




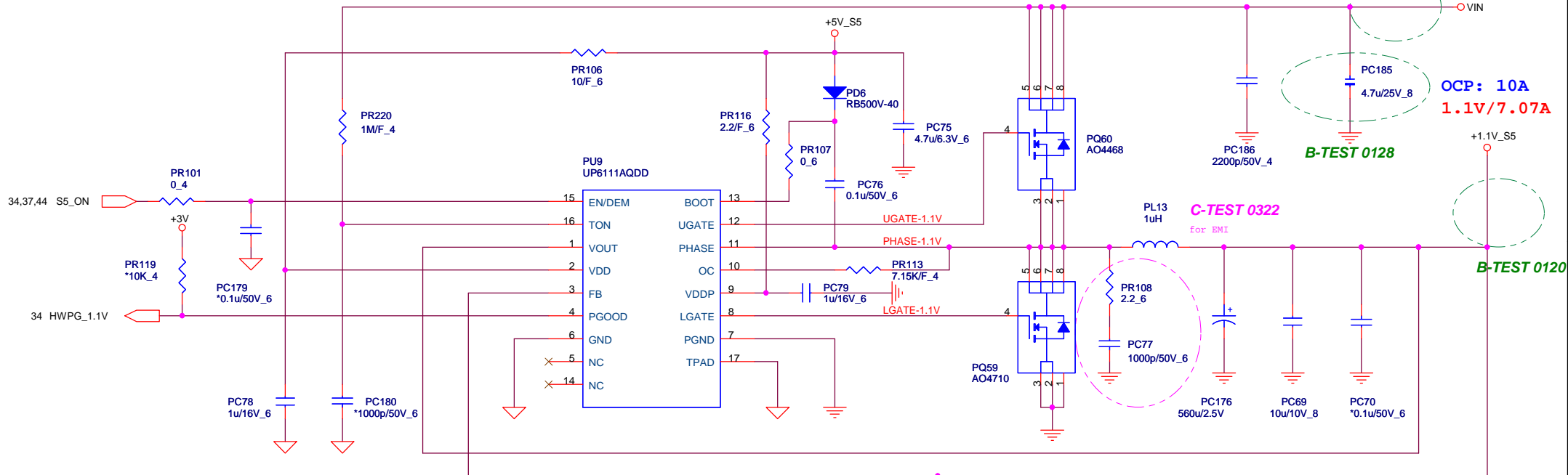




| SVC | SVD | Output |
|-----|-----|--------|
| 0   | 0   | 1.4    |
| 0   | 1   | 1.2    |
| 1   | 0   | 1.0    |
| 1   | 1   | 0.8    |







$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

AO4710  $R_{dson} = 11.7 \sim 14.2m\Omega$

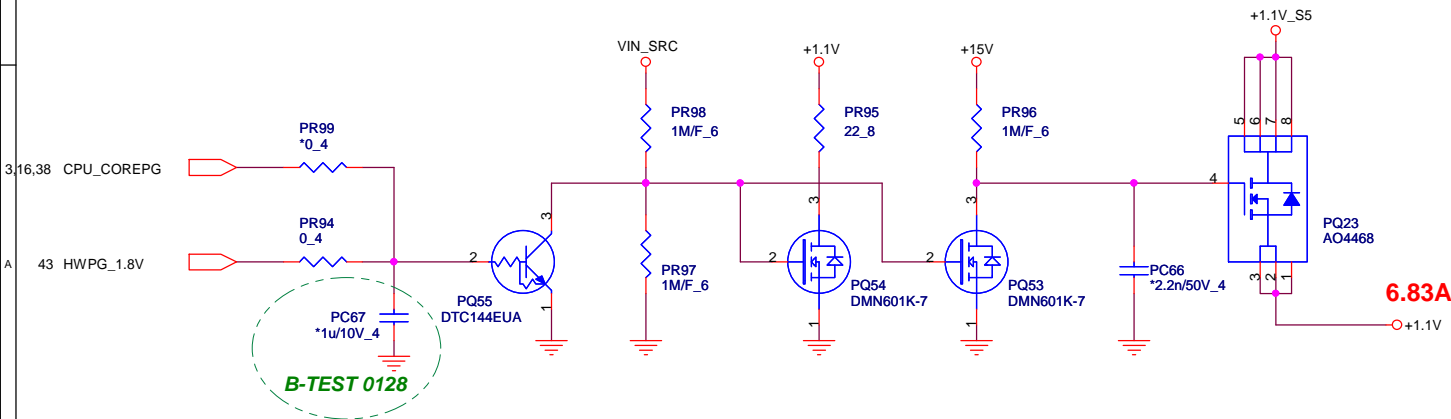
$L(\text{ripple current}) = (19 - 1.1) * 1.1 / (1u * 272k * 19) \sim 3.81A$

$14.2m * 10 = RILIM * 20uA$

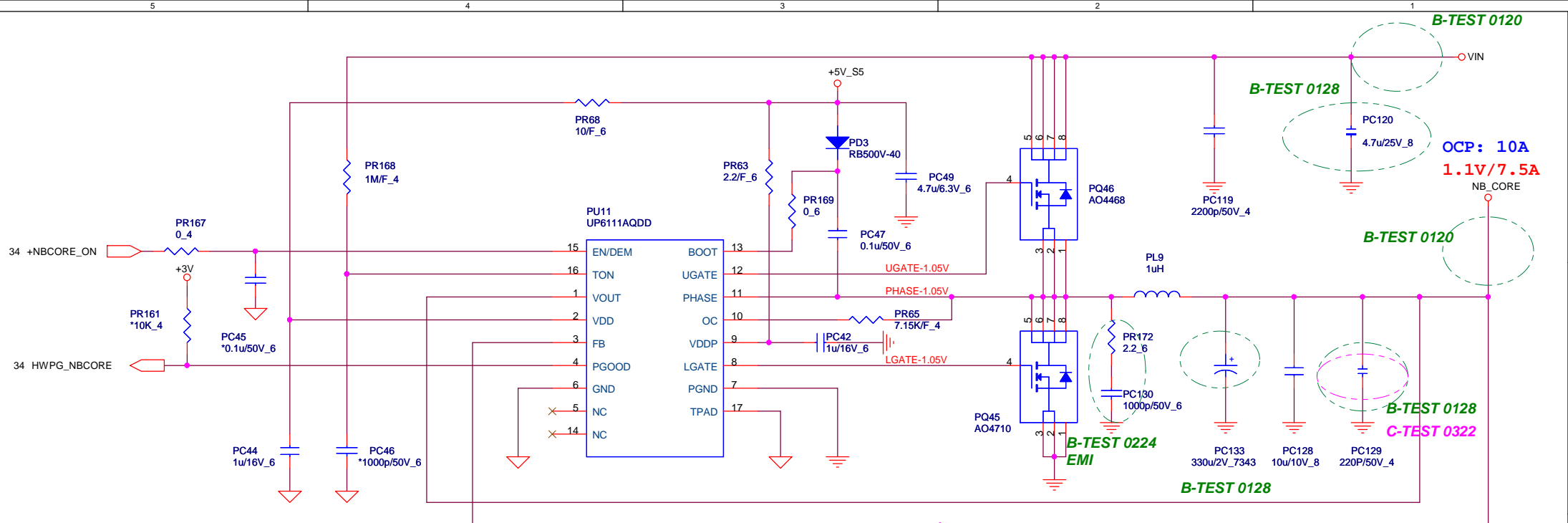
$RILIM = 7.1K \text{ --- } 7.15K$

$$R_{ds} * OCP = RILIM * 20uA$$

$$VOUT = (1 + R1/R2) * 0.75$$







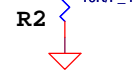
$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

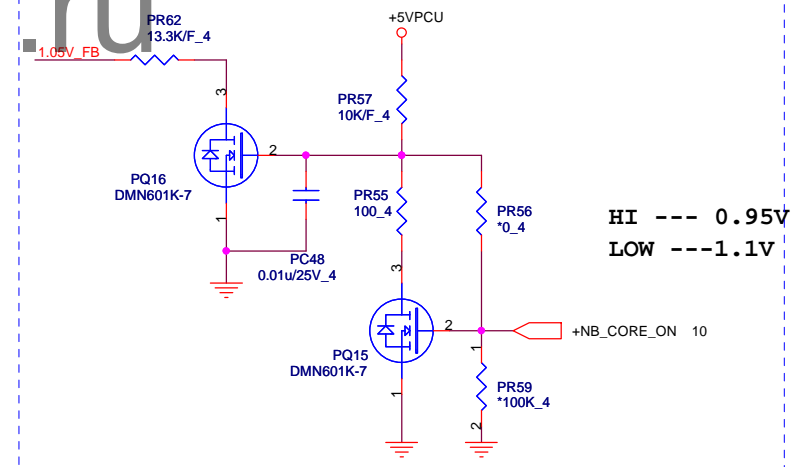
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$$VOUT = (1 + R1/R2) * 0.75$$

stuff PC129 for EMI,  
change footprint from 0603 to 0402  
P/N from \*CH41006K911 to CH12206KB14



AO4710  $R_{dson} = 11.7 \sim 14.2m\Omega$   
 $L(\text{ripple current}) = (19 - 1.05) * 1.05 / (1u * 272k * 19) \sim 3.646A$   
 $14.2m * 10 = RILIM * 20uA$   
 $RILIM = 7.1K \text{ --- } 7.15K$



$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$



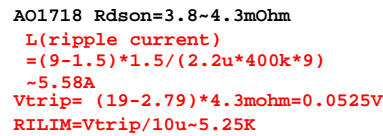
Quanta Computer Inc.

PROJECT : ZRA

| Size | Document Number  | Rev |
|------|------------------|-----|
|      | NB_CORE(UP6111A) | 1A  |

Date: Monday, March 29, 2010 Sheet 40 of 48



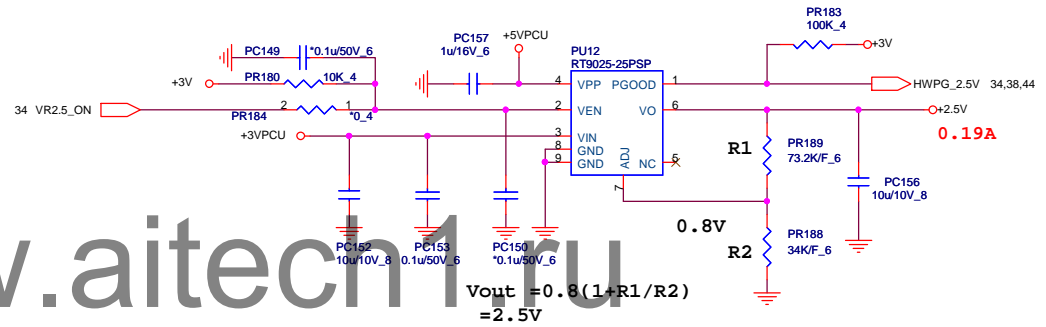
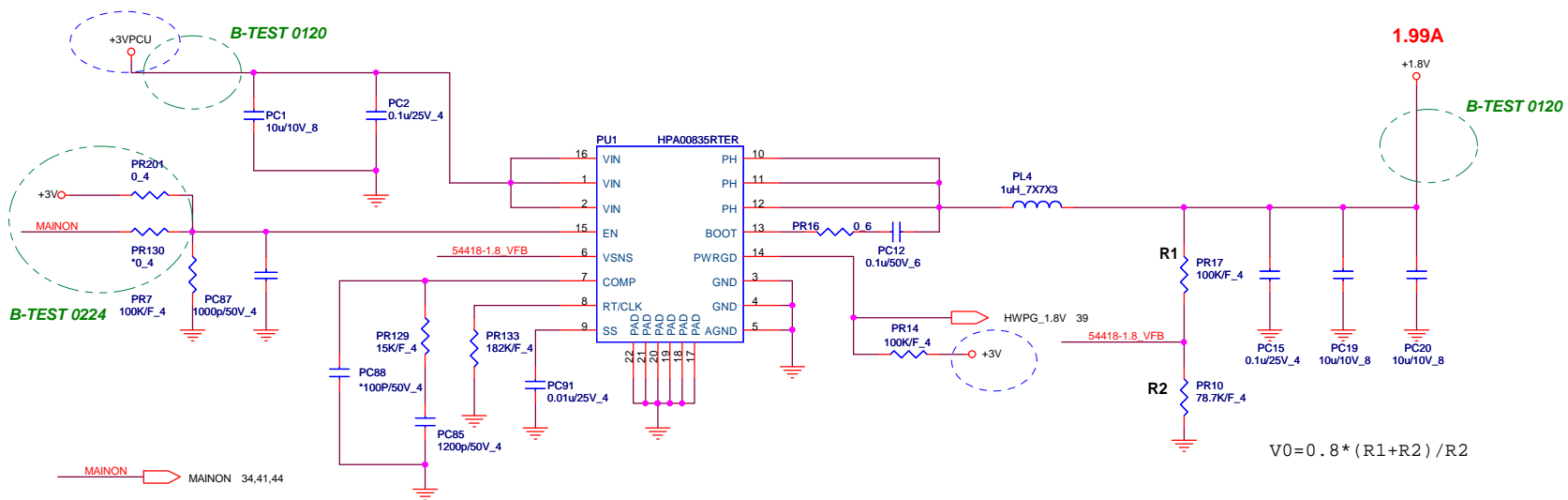


|       | S3 | S5 | +1.5VSUS | REF | VTT |
|-------|----|----|----------|-----|-----|
| S0    | 1  | 1  | ON       | ON  | ON  |
| S3    | 0  | 1  | ON       | ON  | OFF |
| S4/S5 | 0  | 0  | OFF      | OFF | OFF |

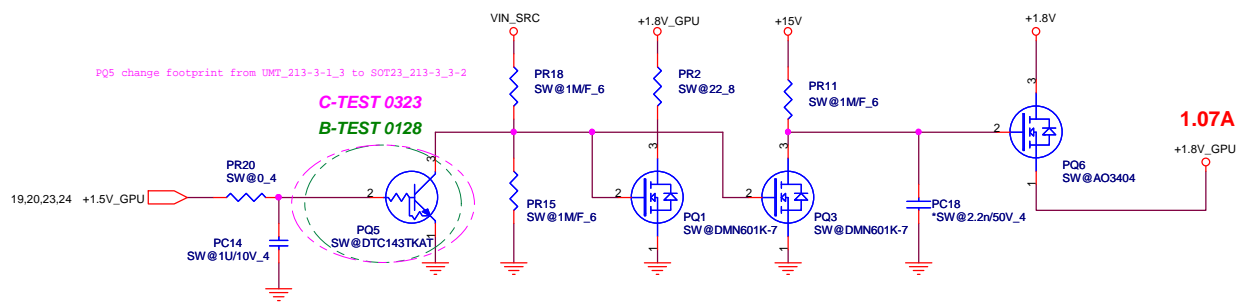
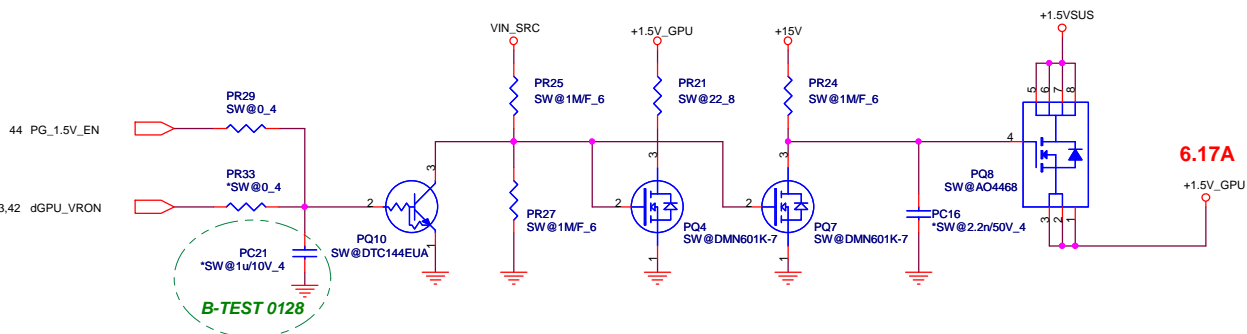




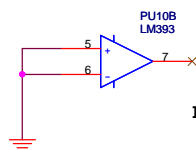
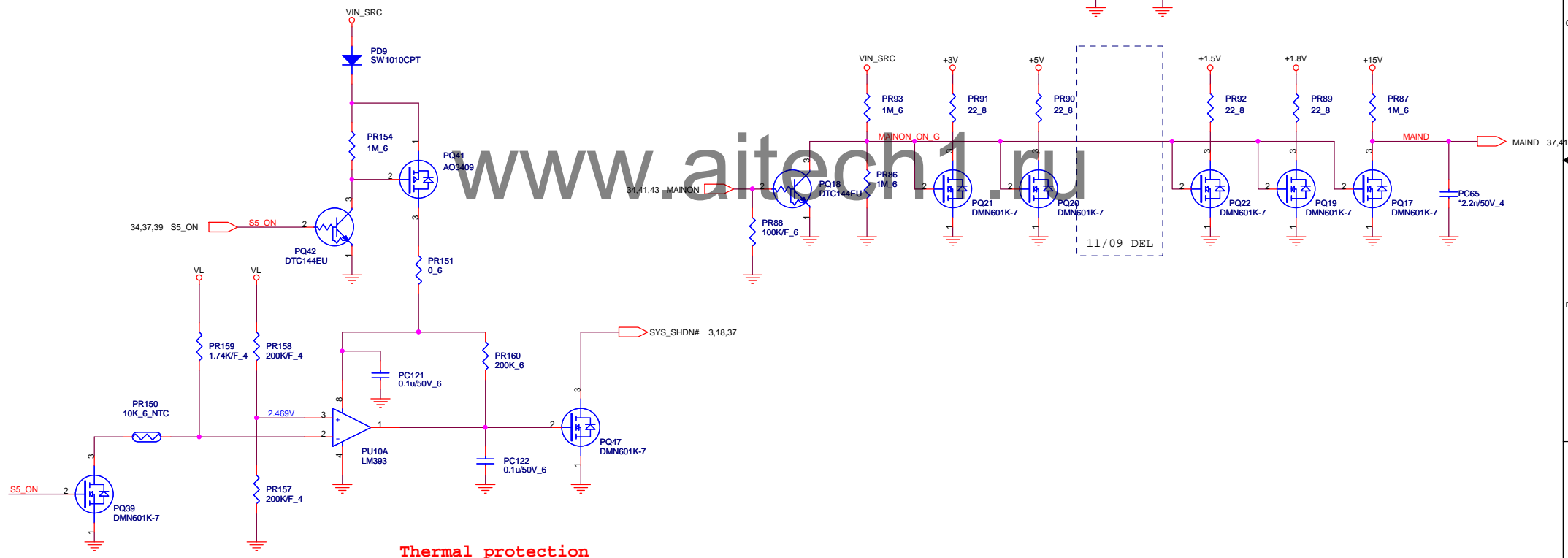
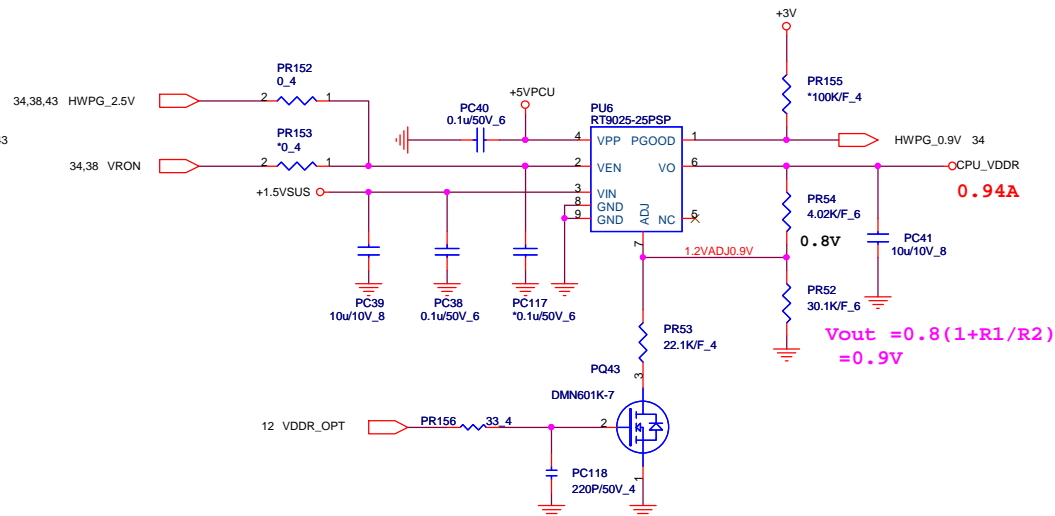
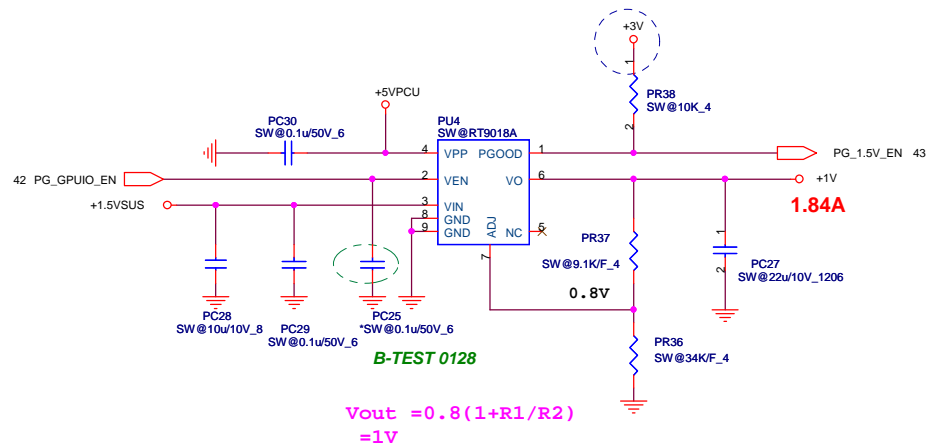




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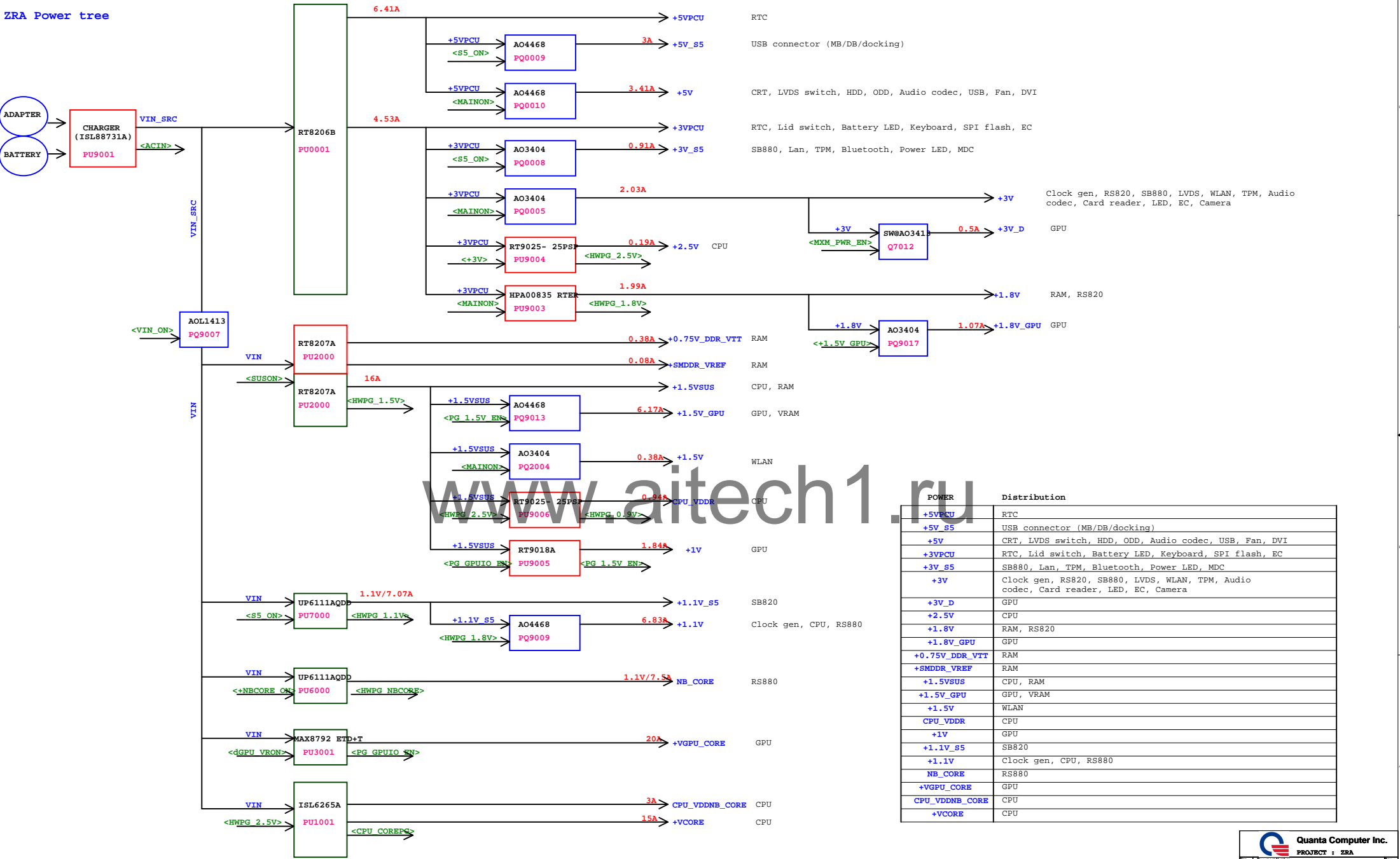




For EC control thermal protection (output 3.3V)



ZRA Power tree



| POWER           | Distribution  |
|-----------------|---|
| +5VPCU          | RTC   |
| +5V_S5          | USB connector (MB/DB/docking)   |
| +5V             | CRT, LVDS switch, HDD, ODD, Audio codec, USB, Fan, DVI                              |
| +3VPCU          | RTC, Lid switch, Battery LED, Keyboard, SPI flash, EC                               |
| +3V_S5          | SB880, Lan, TPM, Bluetooth, Power LED, MDC  |
| +3V             | Clock gen, RS820, SB880, LVDS, WLAN, TPM, Audio codec, Card reader, LED, EC, Camera |
| +3V_D           | GPU   |
| +2.5V           | CPU   |
| +1.8V           | RAM, RS820  |
| +1.8V_GPU       | GPU   |
| +0.75V_DDR_VTT  | RAM   |
| +SMDDR_VREF     | RAM   |
| +1.5VSUS        | CPU, RAM  |
| +1.5V_GPU       | GPU, VRAM   |
| +1.5V           | WLAN  |
| CPU_VDDR        | CPU   |
| +1V             | GPU   |
| +1.1V_S5        | SB820   |
| +1.1V           | Clock gen, CPU, RS880   |
| NB_CORE         | RS880   |
| +VGPU_CORE      | GPU   |
| +CPU_VDDNB_CORE | CPU   |
| +VCORE          | CPU   |



| Model | REV | DATE  | CHANGE LIST   | NOTE        |
|-------|-----|-------|---|-------------|
| ZRA   | A1A | 11/24 | 1.Change Hole31___P29(unguard hole)<br>2.Change CN9009___P32(ME modify T/B connector from 6pin to12 pin)<br>3.Del R7528 ∙ R7529___P28(for all acer project in 2010=>short the WLAN_LED and WWAN_LED)  | ECN Release |
|       |     | 11/25 | 1.Add power tree___P46<br>2.Change CN7019 footprint___P29(NEW=>sata-c166h2-12204-l-22p-r)<br>3.Change PC9064 ∙ PR9021 ∙ PR9025 P/N___P37(PC9064=>CH5104K1900 ∙ PR9021=>CS41502JB10 ∙ PR9025=>CS33902JB01)<br>4.Stuff R7118 ∙ R7115___P11 (for NB REV:11 use )<br>5.Exchange R7105 ∙ C7228___P20(reference AMD design)<br>6.Del U7033A PINAA4 fuction___P13(reference AMD design)<br>7.Rename U7033A PINAJ6 net name___P13(reference AMD design, change from PG_GPUIO_ENA to dGPU_PWROK)                                   |             |
|       |     | 11/26 | 1.Change R7029___P20(AMD suggest change from 1k to 10k)<br>2.no stuff R7060___P19<br>3.Change R7061 ∙ R7070 ∙ R7032___P18(AMD suggest change from 1k to 10k)<br>4.Change R7108 ∙ R9038___P18(AMD suggest change from 1k to 0R)<br>5.no stuff R7029___P20<br>6.Change GPU_VID1 net___P19(change from U7022B PIN AK14 to AM13)<br>7.Change GPU_VID2 net___P19(change from U7022B PIN AM13 to AL13)<br>8.Modify Board ID schematic___P13 ∙ P15(follow ZR8_B)<br>9.Add LED4 ∙ R9252 ∙ RV5___P33(SATA LED movie from DB to MB) |             |
|       |     | 11/27 | 1.Change R9629 footprint___P28(from 0603 to 0402)<br>2.Change CN7022 H___P28(from H=5.6 to H=7)<br>3.Change PJ2 battery footprint___P37(new => bat-bhp-08afeb-8p-l-v)<br>4.Change PR3013 ∙ PR3017 ∙ PR3010 value___P43  |             |
|       |     | 12/01 | 1.Change L7031 ∙ L7060 ∙ L7026 ∙ L7035 ∙ L7032 ∙ L7061 ∙ L7021 ∙ L7033 value___P28(change to PBY160808T-221Y-N)<br>2.Modify Power tree  |             |
|       |     | 12/03 | 1.Change L9000 footprint___P27(from 0806 to 0805)<br>2.Change CN9007 P/N___P30(from DFHD12MS788 to DFHD12MS621)   |             |
|       |     | 12/08 | 1.Change C7343 value_P6(from 1000P to 2200P)<br>2.Change C9098 ∙ C9119 ∙ C9120 ∙ C9121 ∙ C9122 ∙ C9123 value_P34(from 0.1u/10V to 0.1u/25V)<br>3.Change R7437 value_P11(from 140 ohm to 133ohm ==> AMD suggest use docking need matching 133 ohm )  |             |
|       |     | 12/09 | 1.Change C7063 value_P21(from SPE@ to SW@)<br>2.Change C7404 value_P23(from SPE@ to SP@)<br>2.Add R9253_P33   |             |
|       |     | 12/11 | 1.rename<br>2.Change PC24 P/N_P37(from CH5104K1900 to CH5104K9906)<br>3.Change PC55 ∙ PC56 ∙ PC57 ∙ PC58 ∙ PC139 ∙ PC140 P/N_P6/P39(from CH733RM8802 to CH733RY8802)<br>4.Change PL11 P/N_P39(from DC+18V0MZ04 to CV+18V0MZ04 )<br>5.Change LED2 footprint_P33(change to led1tst-s326kgjskt-3p-nb4)   |             |
|       |     | 12/15 | 1.Change CN6 P/N_P32(from DFFC04FR014 to DFFC04FR018)<br>2.DEL R384 ∙ LED6 ∙ RV7_P33(DEL BLUETOOTH LED function)<br>3.Add T100_P33  |             |
|       |     | 12/16 | 1.Add Hole NUT P/N_P32<br>2.DEL CN20 PIN73/PIN74_P36(change from GND to NA)   |             |
|       |     | 12/28 | 1.Modify power sequence_P2<br>2.Modify power tree_P46   |             |
|       |     | 01/20 | 1.Del JP15 ∙ JP16 ∙ JP20 ∙ JP21___P37<br>2.Del JP14 ∙ JP13 ∙ JP12 ∙ RP201 ∙ RP213 ∙ RP209 ∙ RP210___P38<br>3.no stuff PC141___P38<br>4.Change PL12 P/N to CV-2280MZ05 ∙ footprint to CHOKE-PCMC063T-3R3MN-smt___P38<br>5.Change PC154 and PC138 P/N to CC71004MZ01 and Value from 27uF to 100uF___P38<br>6.Del JP19 ∙ JP17 ∙ JP18___P39<br>7.Del JP7 ∙ JP8 ∙ JP10___P40<br>8.Del JP6 ∙ JP9 ∙ JP11___P41<br>9.no stuff PR165___P41<br>10.stuff PR70___P41<br>11.Del JP3 ∙ JP4 ∙ JP5___P42<br>12.Del JP2 ∙ JP1___P43        |             |
|       |     |       |   |             |
|       |     |       |   |             |

B1A



| Model | REV | DATE  | CHANGE LIST  | NOTE        |
|-------|-----|-------|--|-------------|
| ZRA   | B1A | 01/28 | 1.Change Q9 P/N to BAM700200F6___P20<br>2.Change PC17 footprint to 0603 ___P36<br>3.Change PC11 Value from 10uF to 4.7uF , footprint form 1206 to 0805 , P/N from CH61004M291 to CH5474KEA06 ___P36<br>4.Change PC169 、PC173 Value from 10uF to 4.7uF , footprint form 1206 to 0805 , P/N from CH61004M291 to CH5474KEA06 ___P37<br>5.Change PC158 、PC62 、PC142 、PC143 、PC135 、PC136 Value from 10uF to 4.7uF , footprint form 1206 to 0805 , P/N from CH61004M291 to CH5474KEA06 ___P38<br>6.Change PC185 Value from 10uF to 4.7uF , footprint form 1206 to 0805 , P/N from CH61004M291 to CH5474KEA06 ___P39<br>7.no stuff PC67___P39<br>8.Change PC120 Value from 10uF to 4.7uF , footprint form 1206 to 0805 , P/N from CH61004M291 to CH5474KEA06 ___P40<br>9.no stuff PC129___P40<br>10.Change PC114 Value from 10uF to 4.7uF , footprint form 1206 to 0805 , P/N from CH61004M291 to CH5474KEA06 ___P41<br>11.no stuff PC21___P43<br>12.no stuff PC25___P44<br>13.Change PQ5 P/N from BA144EUAZ04 to BA001430Z31___P43<br>14.Change PC133 Value from 560uF to 330uF , footprint form ECAP6_3X6_1-7_2 to CC7343 , P/N from CC7560JMJ215 to CH733RY8802 ___P40<br>15.Change PC106 Value from 560uF to 330uF , footprint form ECAP6_3X6_1-7_2 to CC7343 , P/N from CC7560JMJ215 to CH733RY8802 ___P42<br>16.no stuff R148 、R144___P10<br>17.Del Clock Generator ___P3<br>18.Del R166 、R163 、R162 、R165 、RP21 ___P10<br>19.Del RP26 、RP14 、RP13 、RP27 、RP33 、RP30 、RP29 ___P12<br>20.Del R274 、R297 ___P13<br>21.Change R289 from 100K to 10K ___P13<br>22.Change C687 、C686 from 18P to 27P ___P18<br>23.no stuff R428 、R429___P22<br>24.Modify DDR3 Memory Aperture size table___P22<br>25.Add F1___P25<br>26.Change L32 、L38 、L40 from BLM18BA470SN1 to BLM18BA220SN1D ___P25<br>27.Change R80 from 1.24K to 1.21K ___P26<br>28.Change U14 footprint to soic8-8-1_27-at45db011d ___P26<br>29.Change R60 from 100K to 10K ___P26<br>30.Del R2 ___P26<br>31.Del R593 ___P27<br>32.Modify CN16 schematic ___P30<br>33.Change D10 P/N to BCRB500VZ29 ___P34<br>34.Change CN20 footprint to DOCK-SP07-10207-19-64P-H-SMT ___P35 | ECN Release |
|       |     | 01/29 | 1.Change C797 、C798 from 22P to 27P ___P12<br>2.Change CN13 footprint to rj45-130452-g-12p-v , P/N to DFTJ12FR154___P26<br>3.Change C843 、C846 from 12P to 18P ___P27<br>4.Change U35 PIN21 netname to LPC_CLK0___P27  |             |
|       |     | 02/01 | 1.Add R162___P12<br>2.Del R90 ___P17<br>3.no stuff R76 、R83 、R91 、R45___P17<br>4.Add C494 、U34___P25<br>5.Add CN27___P29<br>6.Del L43 、L45 、L81 、L82 、L66 、L67___P29<br>7.stuff R225 、Q17 (Del IV)___P35<br>8.Add CN28 、L91 、L92 、L93 、L83 、L84 、L88 、C785 、C786 ___P35<br>9.Modify CN20 netname___P35<br>10.stuff R43 ___P17  |             |
|       |     | 02/02 | 1.Add R384___P15<br>2.Add R554___P29   |             |
|       |     | 02/05 | 1.Add Q43 、Q42 、Q44 ___P5<br>2.Add F2 、F3 ___P35   |             |
|       |     | 02/08 | 1.Modify R256 schematic to U17 PIN2___P30  |             |
|       |     | 02/10 | 1.change L77 P/N to CX163210007 , foot print to CHOKE-WCM3216-4P___P35<br>2.Add C495 、C498___P31<br>3.no stuff C441 、C446 、C476 、C475 、C478 、C477___P35<br>4.change CN28 PIN13 、PIN14 from GND to NC___P35<br>5.change CN27 PIN13 、PIN14 from GND to NC___P29<br>6.Change L32 、L38 、L40 P/N from BLM18BA220SN1D to BLM18BA470SN1___P25<br>7.Change C377 、C363 、C351 、C349 、C365 、C376 value from 10p to 6.8p , P/N to CH-6806TB01___P25<br>8.add C796 、C502 、C506 、C522 、C792 、C794 ___P35<br>9.change L78 、L79 、L80 P/N to CX8BA470003___P35  |             |



| Model | REV | DATE  | CHANGE LIST  | NOTE        |
|-------|-----|-------|--|-------------|
| ZRA   | B1A | 02/10 | 10.Add C812、C816、C817、C824、C825、C830____P29<br>11.Add C834____P29<br>12.Add C831、C837、C836、C838、C862、C863、C864、C865、C869、C870、C871____P33<br>13.Add C866、C867____P31<br>14.Change R292,R364,R367,R286,R293,R287,C610,C537 footprint to short pad____P29<br>15.Add C868____P33  | ECN Release |
|       |     | 02/11 | 1.Add C872____P31<br>2.Add R90____P32  |             |
|       |     | 02/21 | 1.Change netname LPC_CLK1 to LPC_CLK0____P34<br>2.no stuff R540、R536、C782、C474、U31____P3<br>3.no stuff RP20____P27   |             |
|       |     | 02/23 | 1.Change R308、R311 from 5.1R to 39R____P29<br>2.Change R71 from 0 ohm to 4.7k ohm and not stuff R71____P20<br>3.Change L78、L79、L80 from BEAD 47R TO 0R____P35<br>4.Change L91、L88、L92、L93、L84、L83 from BEAD 120R TO 0R____P35<br>5.No stuff R262、R257、Y3、C496、C497、and stuff R261、R256____P30<br>6.stuff R292、R364、R367、R286、R293、R287、C610、C537 to 0R____P29<br>7.ADD PC190 10pF____P41<br>8.No stuff PC125____P41<br>9.change PR226 from 143K => 182k、放宽OCP的點____P37<br>10.change PR60 from 5.23K => 6.1k、放宽OCP的點____P41<br>11.change R339、R340 to L66、L67、and change value from 0R to BEAD____P29 |             |
|       |     | 02/25 | 1.No stuff PR178____P41<br>2.change R130 from 2.2K => 300R、Accord with LDT riss time SPEC____P10<br>3.change U15 P/N from AL003257K28 to ALBT3257K18____P25  |             |
|       |     | 02/26 | 1.NO stuff R331 (不分BAP/BXP)____P12   |             |
|       |     | 03/22 | 1.change R175 0ohm to bead(CX8PG221003) and C339 from 0.1uF to 2.2uF(CH52201K991), for monitor noise issue.____P10   |             |

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